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Signed at Osaka, Japan
Date: February 2, 2005

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[DOCUMENT NAME] Patent Application
[FILE NUMBER] 99J03803
[DATE OF FILING] March 10, 2000
[DESTINATION] Commissioner of Patent Office
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[INTERNATIONAL CLASS] G02F 1/133
[TITLE OF THE INVENTION] DATA TRANSFER METHOD, IMAGE DISPLAY DEVICE, AND SIGNAL LINE DRIVING CIRCUIT
[THE NUMBER OF CLAIMS] 15
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[SUM OF PAYMENT] ¥21,000
[LIST OF DOCUMENTS SUBMITTED]
[DOCUMENT NAME] Specification 1
[DOCUMENT NAME] Drawing 1
[DOCUMENT NAME] Abstract 1
[GENERAL POWER OF ATTORNEY NUMBER] 9003082
[PROOF: REQUIRED/UNREQUITED] Required

[TITLE OF DOCUMENT] SPECIFICATION

[TITLE OF THE INVENTION] DATA TRANSFER METHOD, IMAGE DISPLAY DEVICE, AND SIGNAL LINE DRIVING CIRCUIT

[CLAIMS]

[CLAIM 1]

A data transfer method in which scanning lines in a row direction and signal lines in a column direction are formed in a matrix pattern, and a data signal which corresponds to a position on the matrix is applied within one horizontal period to a signal line which corresponds to this position, the signal lines being divided into a plurality of blocks and being sequentially conducted for each line per block so as to transfer the data signal between a matrix section and a data transfer section with respect to each block,

said method characterized by comprising the step of,

with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, the blocks BL1 and BL2 having adjacent signal lines

SL1 and SL2, respectively:

conducting the SL2 as preliminary conduction within one horizontal period prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

[CLAIM 2]

A data transfer method for an image display device having scanning lines in a row direction and signal lines in a column direction which are formed in a matrix pattern and displaying an image according to a data signal by a pixel on the matrix, the method applying a data signal which corresponds to a position on the matrix to a signal line which corresponds to this position within one horizontal period, the signal lines being divided into a plurality of blocks, and the data signal being transferred per block from a data transfer section to the pixel by sequentially inverting a polarity of a potential of the signal line for each line per block with respect to a reference voltage,

said method characterized by comprising the step of,

with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of

the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, the blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, respectively:

inverting a polarity of a potential of the SL2 as preliminary conduction with respect to the reference voltage within one horizontal period, prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

[CLAIM 3]

The method as set forth in claim 1 or 2, wherein the signal lines of the plurality of blocks are simultaneously conducted within said one horizontal period prior to the time the application of the data signal to the BL1 is finished.

[CLAIM 4]

The method as set forth in claim 1 or 2, wherein, during the preliminary conduction of the BL2, the signal line BL2 which is being preliminarily conducted receives a data signal having intermediate intensity between a maximum value and a minimum value of data signals which are applied to the signal lines.

[CLAIM 5]

The method as set forth in claim 1 or 2, wherein the preliminary conduction of the BL2 is carried out during the normal conduction period of the BL1 within said one horizontal period.

[CLAIM 6]

The method as set forth in claim 5, wherein the preliminary conduction of the BL2 is finished at the time when the normal conduction of the BL1 is finished within said one horizontal period, and normal conduction of the BL2 is carried out continuously thereafter.

[CLAIM 7]

A data transfer method in which scanning lines in a row direction and signal lines in a column direction are formed in a matrix pattern, and a data signal which corresponds to a position on the matrix is applied within one horizontal period to a signal line which corresponds to this position, the signal lines being divided into a plurality of blocks and being sequentially conducted for each line per block so as to transfer the data signal between a matrix section and a data transfer section,

said data transfer method being characterized in that:

when input data of one block, equivalent of n signal

lines, which are continuously inputted in a time sequential manner are sampled in n sampling sections and respectively stored as n sampling data, and are outputted to their corresponding signal lines, and

when the n sampling sections are divided into groups, and

when one of the blocks in which order of sampling the input data with respect to a single scanning line is second or after is BL2, and

when a group having a sampling section to which first sampling data Db1 of the block BL2 is inputted is GRa,

said method comprises the step of creating a blank sampling section for storing the sampling data Db1 in the group GRa, after the group GRa stores sampling data of a block in which a sampling time is earlier than the block BL2 with respect to the single scanning line, and before, at the latest, the sampling data Db1 is inputted.

[CLAIM 8]

The method as set forth in claim 7, wherein:

with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of

the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2,

each of said sampling sections has a plurality of systems for storing the sampling data, and

the sampling data of the block BL1 are respectively stored in one of the plurality of systems in each sampling section in a group GR1, and

upon finishing the storage, another storage is started in another group with respect to next sampling data, and then the systems are switched in the group GR1 for the next storage to a system which does not currently store data, before storage of sampling data of the block BL2 is started in the group GR1.

[CLAIM 9]

The method as set forth in claim 7, wherein when a group GR1 is one of the groups, sampling data stored in the group GR1 are outputted after they are stored at least in the group GR1, and while storing sampling data in another group.

[CLAIM 10]

A data transfer method in which scanning lines in a row direction and signal lines in a column direction are

formed in a matrix pattern, and a data signal which corresponds to a position on the matrix is applied within one horizontal period to a signal line which corresponds to this position, the signal lines being divided into a plurality of blocks and being sequentially conducted for each line per block so as to transfer the data signal between a matrix section and a data transfer section,

said data transfer method characterized by comprising the step of,

with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, said blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, respectively:

starting the application of the data signal to the SL2 within one horizontal period, prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

[CLAIM 11]

A data transfer method for an image display device having scanning lines in a row direction and signal lines

in a column direction which are formed in a matrix pattern and displaying an image according to a data signal by a pixel on the matrix, said method applying a data signal which corresponds to a position on the matrix to a signal line which corresponds to this position within one horizontal period, the signal lines being divided into a plurality of blocks, and the data signal being transferred per block from a data transfer section to the pixel by sequentially inverting a polarity of a potential of the signal line for each line per block with respect to a reference voltage, said data transfer method characterized by comprising the step of,

with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, said blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, respectively:

starting the application of the data signal to the SL2 within one horizontal period, prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

[CLAIM 12]

An image display device having scanning lines in a row direction and signal lines in a column direction which are formed in a matrix pattern and applying a data signal which corresponds to a position on the matrix to a signal line which corresponds to this position within one horizontal period, the signal lines being divided into a plurality of blocks, said image display device displaying an image according to the data signal by a pixel on the matrix by transferring the data signal per block from a data transfer section to the pixel on the matrix by sequentially inverting a polarity of a potential of the signal line for each line per block with respect to a reference voltage,

said image display device characterized in that:

the data signal is transferred from the data transfer section to the pixels on the matrix using the data transfer method according to any one of claims 1 through 11.

[CLAIM 13]

A signal line driving circuit which functions as the data transfer section to transfer the data signal to the image display device of claim 12,

said signal line driving circuit characterized in that:

when input data of one block, equivalent of n signal lines, which are continuously inputted in a time sequential manner are sampled in n sampling sections and respectively stored as n sampling data, and outputted to their corresponding signal lines, and

when the n sampling sections are divided into groups, and

when one of the blocks in which order of sampling the input data with respect to a single scanning line is second or after is BL2, and

when a group having a sampling section to which first sampling data Db1 of the block BL2 is inputted is GRa,

said signal line driving circuit generates a group control signal for specifying a timing of creating a blank sampling section for storing the sampling data Db1 in the group GRa, after the group GRa stores sampling data of a block in which a sampling time is earlier than the block BL2 with respect to the single scanning line, and before, at the latest, the sampling data Db1 is inputted.

[CLAIM 14]

The signal line driving circuit as set forth in claim 13,

wherein:

with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and when a block for which the application of the data signal is finished later is BL2,

each of said sampling sections has a plurality of systems for storing the sampling data, and

the sampling data of the block BL1 are respectively stored in one of the plurality of systems in each sampling section in a group GR1, and

upon finishing the storage, and before another storage is started in another group with respect to next sampling data, said signal line driving circuit generates a signal as the group control signal for specifying a timing of switching the systems in the group GR1 for the next storage to a system which does not currently store data, before storage of sampling data of the block BL2 is started in the group GR1.

[CLAIM 15]

The signal line driving circuit as set forth in claim 13, wherein when a group GR1 is one of the groups, said

signal line driving circuit generates a signal as the group control signal for specifying a timing of outputting the sampling data stored in the group GR1, after they are stored at least in the group GR1, and while storing sampling data in another group.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[INDUSTRIAL FIELD OF THE INVENTION]

The present invention relates to a data transfer method for carrying out data transfer using a matrix substrate such as an active-matrix substrate used in liquid crystal display devices and the like, and relates also to image display devices, and signal line driving circuits.

[0002]

[PRIOR ART]

There have been used a variety of data transfer devices which exchange data between elements, such as a display section or a photo-receiving section where signal lines and scanning lines are provided in a matrix pattern, and other elements.

[0003]

For example, active-matrix substrates used in display devices such as a liquid crystal display device

have signal lines for supplying display signals to pixels, and scanning lines for driving a switching element provided for each pixel. In order to drive these signal and scanning lines, external driving circuits (signal line driving circuit, scanning line driving circuit) are installed.

[0004]

Conventionally, the external driving circuits were provided with the same number of output terminals as the number of signal lines and scanning lines for driving these lines. However, attempts have been made to reduce the number of components of the external circuit and to reduce the cost of installing it, by a method in which the number of ICs is reduced to half or one-third, and signals are supplied selectively by signal line switching elements by branching the ICs. For example, in a method disclosed in *Tokukaihei* 8-234237, scanning lines are divided into blocks, and the blocks to which the scanning signals are destined are switched in time so that the scanning lines are sequentially applied to each block by dividing one vertical period with respect to time.

[0005]

[PROBLEMS TO BE SOLVED BY THE INVENTION]

The foregoing conventional structure, however, had a

problem that an error occurred on transfer data by the application of a potential on a signal line at a border line while the potential of the signal line is being oscillated by a parasitic capacitance which exists between the signal line and adjacent signal lines.

[0006]

For example, in the case of a display device, there is a problem that the signal line and pixels which correspond to the border of the blocks are oscillated at the time of switching the blocks by the parasitic capacitance between the signal line and the pixel electrodes. The following explains this principle with reference to a timing chart of Fig. 26, and Fig. 1 which shows a structure according to the present invention. Note that, in reality, there are many other signal lines and their corresponding elements other than those shown in the drawing, which, however, are omitted here for convenience of explanation. The following explanation is based on the case where signals of maximum amplitude are outputted from output lines s_1 to s_4, which respectively correspond to output terminals of the signal line driving circuit 1, for effecting black display over the entire screen.

[0007]

Signal lines f', f, a, and b make up a single block ("first block" hereinafter), and signal lines c, d, e, and e' makes up another block ("second block" hereinafter). While a scanning line g1 is being selected, a signal is first supplied to the signal lines a and b from the signal line driving circuit 1. The signal is applied to pixels A_1 and B_2 because the scanning line g_1 is selected. Here, no signal is supplied to the signal lines c and d. Then, the signal lines a and b, and the pixels A_1 and B_1 become on hold, and a signal is supplied to the signal lines c and d from the signal line driving circuit 1, which is then applied to pixels C_1 and D_1 because the scanning line g_1 is selected. Note that, even though the same signal is supplied to the signal lines a through d in this example of black display over the entire screen, the signal from the signal line driving circuit 1 is normally switched while one scanning line (g_1) is selected.

[0008]

Here, there exists parasitic capacitance Csd between pixel electrodes and signal lines. Fig. 1 only shows Csd at the pixels A_1, B_1, C_1, D_1 and pixels A_2, B_2, C_2, D_2, there are a number of Csds which equal the number of pixels provided in each signal line, and therefore there are

actually capacitance which cannot be ignored compared with the electrostatic capacitance of the entire signal lines. Here, when the destination of the signal is switched from the first block to the second block, i.e., when SW_2 is selected while SW_1 is non-selected, there occurs polarity inversion of the potential of the signal line s, as shown in Fig. 26. Since the signal line b is capacitively coupled with the signal line c via the pixel electrodes (plurality of pixels, e.g., B_2, in the direction of the signal line c), there is a potential hike of some degree on the signal line b by the polarity inversion of the signal line c. Further, since the scanning line g_1 is being selected, the potential hike is supplied to the pixel B_1, and the scanning line g_1 is switched under this condition. Because the foregoing operation occurs with respect to all scanning lines, only a single line which corresponds to the signal line b in the display of the entire screen is supplied with a voltage which is higher than that for the other pixels, and as a result the line is recognized as a black line.

[0009]

Even though the foregoing explained the driving over two blocks, for example, in the case of driving over four blocks on the entire screen, there is a problem that a total

of three black lines are recognized at the respective borders of the blocks.

[0010]

This problem is also present in devices other than the display device, for example, such as an X-ray sensor. That is, signal lines and scanning lines are provided in a matrix pattern on a substrate, and a photo-detecting section having a photo-detecting elements is provided thereon. X-rays are detected by the photo-detecting section and converted to an electrical signal, which is then transferred to an external display device, etc., via the signal lines. Even in this case, when signals are transferred by dividing the signal lines into blocks as in the foregoing case, there will be an error on transfer data by the application of a potential on a signal line at the border while the potential of the signal line is being oscillated by a parasitic capacitance which exists between the signal line and adjacent signal lines.

[0011]

[MEANS TO SOLVE THE PROBLEMS]

In order to solve the foregoing problems, in a data transfer method of the present invention, scanning lines in a row direction and signal lines in a column direction

are formed in a matrix pattern, and a data signal which corresponds to a position on the matrix is applied within one horizontal period to a signal line which corresponds to this position, the signal lines being divided into a plurality of blocks and being sequentially conducted for each line per block so as to transfer the data signal between a matrix section and a data transfer section with respect to each block, wherein, with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, the blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, respectively, the SL2 is conducted as preliminary conduction within one horizontal period prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

[0012]

With this arrangement, within one horizontal period, at least SL2 among the signal lines of the BL2 is preliminarily conducted prior to the time the application of the data signal to the BL1 as normal conduction is

finished. For example, all the signal lines which belong to the BL2, including the SL2, are conducted. In the case of AC driving where the polarity of the potential of the signal lines is inverted with respect to a reference voltage, the polarity of the potential of at least the SL2 is inverted as the preliminary conduction with respect to the reference voltage, prior to the time the application of the data signal to the BL1 as the normal conduction is finished. That is, within one horizontal period, before conduction of at least one block is finished, a signal line of a block to be conducted next is conducted once. In the case of AC driving, the polarity of the signal line of the BL2 is inverted in advance as preliminary polarity inversion before the normal polarity inversion of the BL1.

[0013]

This causes a potential hike on the block BL1 by the preliminary conduction and the potential oscillates, which, however, is restored by the subsequent normal conduction by which a correct potential is applied to the BL1. Thereafter, the application of the data signal to the BL1 is finished and the BL1 maintains and transfers the data signal based on the correct potential. Therefore, it is possible to effectively prevent an error on transfer data,

which is caused by the application of a potential to the signal line on the border of the blocks while the signal line is experiencing potential oscillation by the parasitic capacitance between the signal line and the adjacent signal line. In the case of a display device, it is possible to prevent the phenomenon in which a potential is applied to the pixels on the border while they are oscillated, which state is then maintained over the display period, thus relieving the drawback of different display states between the border and an area surrounding it, which is caused even when the potentials applied to the border and the surrounding area are the same.

[0014]

For example, during the preliminary conduction of the BL2, to the signal line of the BL2 undergoing the preliminary conduction is applied a signal, which is applied during its normal conduction period while the line is being selected. In this way, the signal line undergoing the preliminary conduction in the BL2 receives the same signal which should be applied in the preliminary conduction period and in the normal conduction period. As a result, there will be no potential difference between the two signals. Accordingly, no potential drop will be

caused by the potential difference on the signal line in the BL1. Thus, in addition to the effect by the foregoing arrangement, it is possible to further relieve the drawback of different potentials between the border and an area surrounding it, even though the same potential is applied to the block and the surrounding area.

[0015]

Further, the data transfer method of the present invention is for an image display device having scanning lines in a row direction and signal lines in a column direction which are formed in a matrix pattern and displaying an image according to a data signal by a pixel on the matrix, the method applying a data signal which corresponds to a position on the matrix to a signal line which corresponds to this position within one horizontal period, the signal lines being divided into a plurality of blocks, and the data signal being transferred per block from a data transfer section to the pixel by sequentially inverting a polarity of a potential of the signal line for each line per block with respect to a reference voltage, wherein, with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of

the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, the blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, respectively, a polarity of a potential of the SL2 is inverted as preliminary conduction with respect to the reference voltage within one horizontal period, prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

[0016]

With this arrangement, within one horizontal period, the polarity of the potential of the SL2 is inverted within one horizontal period as the preliminary conduction with respect to the reference voltage, prior to the time the application of the data signal to the BL1 is finished as the normal conduction for applying the data signal. For example, the polarity of all the signal lines of the BL2, including the SL2, are inverted with respect to the reference voltage. That is, in AC driving where the polarity of the signal lines is inverted with respect to the reference voltage, the polarity of the potential of at least the SL2 is inverted as the preliminary conduction with respect to the reference voltage, prior to the time the application of the

data signal to the BL1 as the normal conduction is finished. That is, within one horizontal period, before the conduction of at least one block is finished, the polarity of the potential of the signal lines of a block which is to be conducted next is inverted with respect to the reference voltage. That is, in AC driving, the polarity of the signal line of the BL2 is inverted in advance as the preliminary polarity inversion before the normal polarity inversion of the BL1.

[0017]

This causes a potential hike on the block BL1 by the preliminary conduction and the potential oscillates, which, however, is restored by the subsequent normal conduction by which a correct potential is applied to the BL1. Thereafter, the application of the data signal to the BL1 is finished and the BL1 maintains and transfers the data signal based on the correct potential. Therefore, it is possible to effectively prevent an error on transfer data, which is caused by the application of a potential to the signal line on the border of the blocks while the signal line is experiencing potential oscillation by the parasitic capacitance between the signal line and the adjacent signal line. In the case of a display device, it is possible to

prevent the phenomenon in which a potential is applied to the pixels on the border while they are oscillated, which state is then maintained over the display period. As a result, it is possible to relieve the drawback of different display states between the border and an area surrounding it, which is caused even when the potentials applied to the border and the surrounding area are the same.

[0018]

Further, the data transfer method of the present invention, in addition to the foregoing arrangement, may have an arrangement wherein the signal lines of the plurality of blocks are simultaneously conducted within one horizontal period prior to the time the application of the data signal to the BL1 is finished.

[0019]

According to this arrangement, the signal lines of the plurality of blocks are conducted within the one horizontal period prior to the time the application of the data signal to the BL1 is finished. In the case of AC driving, the potential of the signal lines of the plurality of blocks are inverted, prior to the application of the data signal to the BL1 is finished, to the opposite polarity with respect to

the reference voltage.

[0020]

Thus, even when driving multiple blocks, since the preliminary conduction period such as the preliminary polarity inversion is common to all blocks, the time required for the preliminary inversion does not become overly long as a whole, thus saving time for the normal conduction such as the normal polarity inversion. This allows the signal to be applied without congestion, thus improving the quality of data transfer process, in addition to the effect by the foregoing arrangement.

[0021]

Further, the data transfer method of the present invention, in addition to the foregoing arrangement, may have an arrangement wherein, during the preliminary conduction of the BL2, a data signal having intermediate intensity between a maximum value and a minimum value of data signals which are applied to the signal lines is applied to the signal line BL2 which is being preliminarily conducted.

[0022]

According to this arrangement, during the preliminary conduction of the BL2, a data signal having

intermediate intensity between a maximum value and a minimum value of data signals which are applied to the signal lines is applied to the signal line BL2 which is being preliminarily conducted. For example, in the case of a display device, to the pixels as the data processing section are applied a halt-tone data signal which is an intermediate of the black display and the white display. As a result, the signal lines in the BL1 will not experience an abrupt potential drop by a small potential difference when the data signal is a half-tone. In general, for example, in the case of a display device, the visibility on a display with respect to a small potential difference becomes most notable when the data signal has an intermediate signal intensity (half-tone) between the maximum value and the minimum value. The foregoing arrangement can effectively prevent a difference in display state even when the difference becomes most notable as in this case. Thus, in addition to the effect by the foregoing arrangement, it is possible to relieve the drawback of different display states between the border and an area surrounding it, which is caused even when the potentials applied to the border and the surrounding area are the same.

[0023]

Further, the data transfer method of the present invention, in addition to the foregoing arrangement, may have an arrangement wherein the preliminary conduction of the BL2 is carried out during the normal conduction period of the BL1 within one horizontal period.

[0024]

According to this arrangement, the preliminary conduction of the BL2 is carried out during the normal conduction period of the BL1 within one horizontal period.

[0025]

Thus, even when driving multiple blocks, since the preliminary conduction period such as the preliminary polarity inversion is common to all blocks, the time required for the preliminary conduction does not become overly long as a whole, thus saving time for the normal conduction such as the normal polarity inversion. This allows the signal to be applied without congestion, thus improving the quality of data transfer process, in addition to the effect by the foregoing arrangement.

[0026]

Further, the data transfer method of the present invention, in addition to the foregoing arrangement, may have an arrangement wherein the preliminary conduction

of the BL2 is finished at the time when the normal conduction of the BL1 is finished within one horizontal period, and normal conduction of the BL2 is carried out continuously thereafter.

[0027]

According to this arrangement, the preliminary conduction of the BL2 is finished at the time when the normal conduction of the BL1 is finished within one horizontal period, and the normal conduction of the BL2 is carried out continuously thereafter. By this shift of the overlapping normal conduction periods of the respective blocks, the normal conduction period of the BL2 (ON period of each control wire) can be regarded as a conduction period which is composed of a preliminary conduction period which overlaps the normal conduction period of the BL1 and a normal conduction period after the normal conduction period of the BL1.

[0028]

Therefore, in practice, this arrangement can be realized only by slightly changing the timing of signals for specifying the start and the end of the normal conduction period, and it is not required to newly create a signal for specifying the start and the end of the preliminary

conduction period. As a result, in addition to the effect by the foregoing arrangement, the arrangement of the device for effecting the foregoing driving can be simplified.

[0029]

Further, in the data transfer method of the present invention, scanning lines in a row direction and signal lines in a column direction are formed in a matrix pattern, and a data signal which corresponds to a position on the matrix is applied within one horizontal period to a signal line which corresponds to this position, the signal lines being divided into a plurality of blocks and being sequentially conducted for each line per block so as to transfer the data signal between a matrix section and a data transfer section, wherein, when input data of one block, equivalent of n signal lines, which are continuously inputted in a time sequential manner are sampled in n sampling sections and respectively stored as n sampling data, and are outputted to their corresponding signal lines, and when the n sampling sections are divided into groups, and when one of the blocks in which order of sampling the input data with respect to a single scanning line is second or after is BL2, and when a group having a sampling section to which first sampling data Db1 of the block BL2

is inputted is GRa, a blank sampling section for storing the sampling data Db1 is created in the group GRa, after the group GRa stores sampling data of a block in which a sampling time is earlier than the block BL2 with respect to the single scanning line, and before, at the latest, the sampling data Db1 is inputted.

[0030]

For example, the n sampling sections can be grouped based on those having the same switching time therein. Further, the n sampling sections can be grouped based on those having the same output time with respect to the data signal which is outputted to one of the blocks of the signal lines.

[0031]

When not grouping, the first to nth data signals are sampled first with respect to the data signal which is outputted to one of the blocks of the signal lines, and thereafter the first to nth signal lines thus sampled are transferred to the signal lines or latched, before sampling the first data signal again. This requires time for the transfer or latching. Thus, when transferring data signals which are in chronological sequence, i.e., data signals which are successively inputted one after another with

certain time intervals, and when the transfer time or latch time cannot be ignored compared with the supply intervals of the data signals, sampling cannot catch up with the data transfer and the data signals are missed out. In other words, it is required to modify the data signals in some way or another, for example, by incorporating an index signal in data signals to be transferred, taking into consideration the transfer time.

[0032]

In contrast, according to the arrangement of the present invention, input data of one block, equivalent of n signal lines, which are continuously inputted in a time sequential manner are sampled in n sampling sections and respectively stored as n sampling data, and are outputted to their corresponding signal lines, and n sampling sections are divided into groups, and when one of the blocks in which order of sampling the input data with respect to a single scanning line is second or after is BL2, and when a group having a sampling section to which first sampling data Db1 of the block BL2 is inputted is GRa, a blank sampling section for storing the sampling data Db1 in the group GRa is created after the group GRa stores sampling data of a block in which a sampling time

is earlier than the block BL2 with respect to the single scanning line, and before, at the latest, the sampling data Db1 is inputted.

[0033]

Therefore, when there are n input lines for the signal lines (accordingly, the number of signal lines is integer multiples of n), it is not required to provide, neither after the nth data signal is sampled nor before the first data signal is sampled again, time for transferring the sampled data signals to the signal lines or latching the same. Accordingly, it is not required to specially modify the data signals according to the transfer time or latch time. As a result, data can be transferred rapidly and processed fast with a simpler structure.

[0034]

The blank sampling section can be created by using and suitably outputting a group control signal which indicates the timing of this operation. Such a group control signal, for example, is the group control signal (system switching timing signal) which, by the provision of a plurality of systems (system A, system B, etc.) for storing data signals in each sampling section, indicates the timing of switching the systems for storing the data

signal to a blank system. Also, for example, such a group control signal is the group control signal (output timing signal) which indicates the timing of outputting the stored sampling data by transferring or latching it while another group is undergoing input and storage operation of other sampling data.

[0035]

Further, the data transfer method of the present invention, in addition to the foregoing arrangement, may have an arrangement wherein, with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, when a block for which the application of the data signal is finished earlier is BL1, and when a block for which the application of the data signal is finished later is BL2, each of the sampling sections has a plurality of systems for storing the sampling data, and the sampling data of the block BL1 are respectively stored in one of the plurality of systems in each sampling section within a group GR1, and upon finishing the storage, another storage is started in another group with respect to next sampling data, and then the systems are switched in the group GR1 for the next storage to a system which does not currently store data,

before storage of sampling data of the block BL2 is started in the group GR1.

[0036]

With this arrangement, with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, when a block for which the application of the data signal is finished earlier is BL1, and when a block for which the application of the data signal is finished later is BL2, each of the sampling sections has a plurality of systems for storing the sampling data, and the sampling data of the block BL1 are respectively stored in one of the plurality of systems in each sampling section within a group GR1, and upon finishing the storage, another storage is started in another group with respect to next sampling data, and then the systems are switched in the group GR1 for the next storage to a system which does not currently store data, before storage of sampling data of the block BL2 is started in the group GR1. The switching is made simultaneously per block.

[0037]

For example, the sampling data are stored per group in one of the plurality of systems of the sampling section,

and upon finishing the storage, the systems are switched simultaneously per block for the next storage to a system which does not currently store data, and the input data, which is inputted while a certain group was undergoing system switching, can be sampled in another group, for example, in a group which is not undergoing system switching at this time.

[0038]

Also, for example, among the data signal for the block BL1, which is sampled before the block BL2, with respect to a single scanning line, the data signal which is sampled last is stored in system A of a certain group, and the first sampling data Db1 of the block BL2 is stored in another group GRa while the former group is being switched to system B. The sampling data which is stored in one system of a group can be outputted while storing sampling data in another system of the group. Alternatively, the output can be made during a period in which no system in the group is storing data.

[0039]

Thus, even though the storage and output are switched between systems by providing plural systems with respect to each signal line within a block, the group

which performs the storage process is switched to ensure sampling of the data signal in another group, thus surely preventing failure to pick up data. Therefore, in addition to the effect by the foregoing arrangement, data can be transferred faster with a simpler arrangement, thereby processing data at high speed.

[0040]

The switching can be made by using and suitably outputting a group control signal which indicates the timing of the switching operation. Such a group control signal is the group control signal (system switching timing signal) which, by the provision of a plurality of systems (system A, system B, etc.) for storing data signals in each sampling section, indicates the timing of switching the system for storing the data signal to a blank system between the systems. The sampling signal is switched in this manner at the timing of the group control signal.

[0041]

Further, the data transfer system of the present invention, in addition to the foregoing arrangement, may have an arrangement wherein when a group GR1 is one of the groups, the sampling data stored in the group GR1 are outputted after it was stored at least in the group GR1,

and while storing sampling data in another group.

[0042]

According to this arrangement, when a group GR1 is one of the groups, the sampling data stored in the group GR1 are outputted after it was stored at least in the group GR1, and while storing sampling data in another group.

[0043]

Thus, even though the storage and output are switched between systems by providing plural systems with respect to each signal line within a block, the group which performs the storage process is switched to ensure sampling of the data signal in another group, thus surely preventing failure to pick up data. Therefore, in addition to the effect by the foregoing arrangement, data can be transferred faster with a simpler arrangement, thereby processing data at high speed.

[0044]

For example, it is possible to have an arrangement wherein while sampling the data signal within a group, the signal which has been sampled in another group is transferred therefrom to the signal lines or latched, and a group control signal which specifies the timing of transfer or latching is outputted. For example, with respect to the

data signals which are outputted to one of the blocks of the signal lines, those which are outputted at the same time are grouped, and, two of the groups, e.g., two groups which output data signals in consecutive order are denoted by GR1, having earlier output time, and GR2, having later output time, respectively, and the data signal can be subsequently outputted per block to one of the blocks of the signal lines by transferring or latching the signal which has been sampled in GR1 to the signal lines while sampling data signals in GR2.

[0045]

The output can be carried out by using and suitably outputting a group control signal which indicates the timing of the output operation. For example, such a group control signal is the group control signal (output timing signal) which indicates the timing of outputting the stored sampling data by transferring or latching it while another group is undergoing input and storage operation of other sampling data. In this manner, the lines of at least two groups are independently controlled by different group control signals. That is, in group GR1, the timing of sampling and the timing of transfer or latching are specified by a group control signal (CNTa), and in group

GR2, the timing of sampling of the timing of transfer or latching are specified by a group control signal (CNTb).

[0046]

Further, in the data transfer method of the present invention, scanning lines in a row direction and signal lines in a column direction are formed in a matrix pattern, and a data signal which corresponds to a position on the matrix is applied within one horizontal period to a signal line which corresponds to this position, the signal lines being divided into a plurality of blocks and being sequentially conducted for each line per block so as to transfer the data signal between a matrix section and a data transfer section, wherein, with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, the blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, respectively, the application of the data signal to the SL2 is started within one horizontal period, prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

[0047]

For example, in the case of AC driving, it is possible to have an arrangement wherein the normal polarity inversion for applying the data signal to the SL2 is started within one horizontal period, prior to the time the normal polarity inversion as the normal conduction for applying the data signal to the BL1 is finished.

[0048]

According to this arrangement, within one horizontal period, the application of the data signal to the SL1 is started prior to the time the application of the data signal to the BL1 is finished as the normal conduction for applying the data signal. That is, the respective signal lines of the BL2 are conducted by starting the normal conduction before the application of the data signal to the BL1 is finished.

[0049]

By this conduction, the block BL1 experiences the potential hike and the potential oscillates, which, however, is restored as and while the data signal is continuously applied to the BL1 for a brief moment after the conduction period. Thereafter, the application of the data signal to the BL1 is finished, and the BL1 can maintain and

transfer the correct potential. Therefore, it is possible to effectively prevent an error on transfer data, which is caused by the application of a potential to the signal line on the border while the signal line is experiencing potential oscillation by the parasitic capacitance between the signal line and the adjacent signal line.

[0050]

In the case of a display device, it is possible to prevent the phenomenon in which a potential is applied to the pixels on the border while they are oscillated, which state is then maintained over the display period. As a result, it is possible to relieve the drawback of different display states between the border and an area surrounding it, which is caused even when the potentials applied to the border and the surrounding area are the same.

[0051]

The conduction is started in advance at an earlier timing than usual to avoid error. This can be realized only be slightly changing the timing of the signal for specifying the start time and the end time of the normal conduction period, and it is not required to newly create a signal for specifying the start time and the end time for the early

conduction, thereby simplifying a device structure for the driving.

[0052]

Further, the data transfer method of the present invention is for an image display device having scanning lines in a row direction and signal lines in a column direction which are formed in a matrix pattern and displaying an image according to a data signal by a pixel on the matrix, the method applying a data signal which corresponds to a position on the matrix to a signal line which corresponds to this position within one horizontal period, the signal lines being divided into a plurality of blocks, and the data signal being transferred per block from a data transfer section to the pixel by sequentially inverting a polarity of a potential of the signal line for each line per block with respect to a reference voltage, wherein, with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, the blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, respectively, the application of the data

signal to the SL2 is started within one horizontal period, prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

[0053]

That is, it is possible to have an arrangement in AC driving wherein, within one horizontal period, the normal polarity inversion for applying the data signal to the SL2 is started prior to the time the normal polarity inversion of the BL1 is finished as the normal conduction for applying the data signal.

[0054]

With this arrangement, the application of the data signal to the SL2 is started within one horizontal period prior to the time the application of the data signal to the BL1 is finished as the normal conduction for applying the data signal. That is, the respective signal lines of the BL2 are conducted in advance by starting the normal conduction before the application of the data signal to the BL1 is finished.

[0055]

By this conduction, the block BL1 experiences the potential hike and the potential oscillates, which, however,

is restored as and while the data signal is continuously applied to the BL1 for a brief moment after the conduction period. Thereafter, the application of the data signal to the BL1 is finished, and the BL1 can maintain and transfer the correct potential. Therefore, it is possible to effectively prevent an error on transfer data, which is caused by the application of a potential to the signal line on the border while the signal line is experiencing potential oscillation by the parasitic capacitance between the signal line and the adjacent signal line.

[0056]

As a result, in a display device, it is possible to prevent the phenomenon in which a potential is applied to the pixels on the border while they are oscillated, which state is then maintained over the display period. As a result, it is possible to relieve the drawback of different display states between the border and an area surrounding it, which is caused even when the potentials applied to the border and the surrounding area are the same.

[0057]

The conduction is started in advance at an earlier timing than usual to avoid error. This can be realized only

be slightly changing the timing of the signal for specifying the start time and the end time of the normal conduction period, and it is not required to newly create a signal for specifying the start time and the end time for the early conduction, thereby simplifying a device structure for the driving.

[0058]

An image display device of the present invention includes scanning lines in a row direction and signal lines in a column direction which are formed in a matrix pattern and applies a data signal which corresponds to a position on the matrix to a signal line which corresponds to this position within one horizontal period, the signal lines being divided into a plurality of blocks, the image display device displaying an image according to the data signal by a pixel on the matrix by transferring the data signal per block from a data transfer section to the pixel on the matrix by sequentially inverting a polarity of a potential of the signal line for each line per block with respect to a reference voltage, wherein the data signal is transferred from the data transfer section to the pixels on the matrix using any of the foregoing data transfer methods.

[0059]

According to this arrangement, the data signal is transferred from the data transfer section to the pixels on the matrix using any of the foregoing data transfer methods. Thus, it is possible to prevent the phenomenon in which a potential is applied to the pixels on the border while they are oscillated, which state is then maintained over the display period. As a result, it is possible to relieve the drawback of different display states between the border and an area surrounding it, which is caused even when the potentials applied to the border and the surrounding area are the same.

[0060]

Further, in a signal line driving circuit of the present invention which functions as the data transfer section to transfer the data signal to the image display device, when input data of one block, equivalent of n signal lines, which are continuously inputted in a time sequential manner are sampled in n sampling sections and respectively stored as n sampling data, and outputted to their corresponding signal lines, and when the n sampling sections are divided into groups, and when one of the blocks in which order of sampling the input data with respect to a single scanning

line is second or after is BL2, and when a group having a sampling section to which first sampling data Db1 of the block BL2 is inputted is GRa, the signal line driving circuit generates a group control signal for specifying a timing of creating a blank sampling section for storing the sampling data Db1 in the group GRa, after the group GRa stores sampling data of a block in which a sampling time is earlier than the block BL2 with respect to a single scanning line, and before, at the latest, the sampling data Db1 is inputted.

[0061]

According to this arrangement, the signal line driving circuit generates a group control signal for specifying a timing of creating a blank sampling section for storing the sampling data Db1 in the group GRa, after the group GRa stores sampling data of a block in which sampling time is earlier than the block BL2 with respect to a single scanning line, and before, at the latest, the sampling data Db1 is inputted.

[0062]

Therefore, when there are n input lines for the signal lines (accordingly, the number of signal lines is integer multiples of n), it is not required to provide, neither after

the nth data signal is sampled nor before the first data signal is sampled again, time for transferring the sampled data signals to the signal lines or latching the same. Accordingly, it is not required to specially modify the data signals according to the transfer time or latch time. As a result, data can be transferred rapidly and processed fast with a simpler structure.

[0063]

Further, the signal line driving circuit of the present invention, in addition to the foregoing arrangement, may have an arrangement wherein with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, when a block for which the application of the data signal is finished earlier is BL1, and when a block for which the application of the data signal is finished later is BL2, each of the sampling sections has a plurality of systems for storing the sampling data, and the sampling data of the block BL1 are respectively stored in one of the plurality of systems in each sampling section within a group GR1, and upon finishing the storage, and before another storage is started in another group with respect to next sampling data, the signal line driving circuit generates a signal as

the group control signal for specifying a timing of switching the systems in the group GR1 for the next storage to a system which does not currently store data, before storage of sampling data of the block BL2 is started in the group GR1.

[0064]

According to this arrangement, with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, when a block for which the application of the data signal is finished earlier is BL1, and when a block for which the application of the data signal is finished later is BL2, each of the sampling sections has a plurality of systems for storing the sampling data, and the sampling data of the block BL1 are respectively stored in one of the plurality of systems in each sampling section within a group GR1, and upon finishing the storage, and before another storage is started in another group with respect to next sampling data, the systems are switched in the group GR1 for the next storage to a system which does not currently store data, before storage of sampling data of the block BL2 is started in the group GR1. The switching is made simultaneously per block.

[0065]

Thus, even though the storage and output are switched between systems by providing plural systems with respect to each signal line within a block, the group which performs the storage process is switched to ensure sampling of the data signal in another group, thus surely preventing failure to pick up data. Therefore, in addition to the effect by the foregoing arrangement, data can be transferred faster with a simpler arrangement, thereby processing data at high speed.

[0066]

Further, the data signal line driving circuit of the present invention, in addition to the foregoing arrangement, may have an arrangement wherein when a group GR1 is one of the groups, the signal line driving circuit generates a signal as the group control signal for specifying a timing of outputting the sampling data stored in the group GR1, after it was stored at least in the group GR1, and while storing sampling data in another group.

[0067]

According to this arrangement, when a group GR1 is one of the groups, the sampling data stored in the group GR1 is outputted after it was stored at least in the group

GR1, and while storing sampling data in another group.

[0068]

Thus, it is not required to switch the storage and output between the systems by providing plural systems with respect to each signal line within a block, and it is not required to provide time for switching. Therefore, in addition to the effect by the foregoing arrangement, data can be transferred faster with a simpler arrangement, thereby processing data at high speed.

[0069]

Further, the data transfer device of the present invention may be used for an image display device which includes scanning lines in a row direction and signal lines in a column direction which are formed in a matrix pattern and applies a data signal which corresponds to a position on the matrix to a signal line which corresponds to this position within one horizontal period, and which displays an image by transferring the data signal to the pixels on the matrix, the signal lines being divided into a plurality of blocks, and the data signal being transferred per block between the matrix section and the data transfer section by sequentially conducting the signal lines for each line per block, wherein, with respect to at least one

pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, and the blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, respectively, the data transfer device includes a conduction control section for conducting the SL2 as the preliminary conduction so as to transfer the data signal from the data transfer section to the pixel on the matrix within one horizontal period, prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

[0070]

According to this arrangement, among the signal lines which belong to the BL2, at least the SL2 is conducted as the preliminary conduction within one horizontal period, prior to the time the application of the data signal to the BL1 is finished as the normal conduction. For example, all the signal lines, including the SL2, which belong to the BL2 are conducted. In the case of AC driving where the polarity of the potential of the signal lines is inverted with respect to the reference

voltage, the polarity of the potential of at least the SL2 is inverted as the preliminary conduction with respect to the reference voltage, prior to the application of the data signal as the normal conduction to the BL1 is finished. Thus, it is possible to prevent the phenomenon in which a potential is applied to the pixels on the border while they are oscillated, which state is then maintained over the display period. As a result, it is possible to relieve the drawback of different display states between the border and an area surrounding it, which is caused even when the potentials applied to the border and the surrounding area are the same.

[0071]

[EMBODIMENTS]

(First Embodiment)

The following will describe one embodiment of the present invention referring to Fig. 1 through Fig. 20. In the present embodiment, a data transfer device is an active-matrix substrate (matrix section), and includes scanning lines, signal lines, and pixel electrodes, which make up a liquid crystal display device as a display device which is driven by the active-matrix mode for display.

[0072]

The pixel electrodes have their respective pixels A_1, B_1, ..., as a data processing section, and are connected to pixel switching elements such as TFTs (Thin Film Transistor) (not shown). The pixels are made up of liquid crystal, which makes up a liquid crystal panel, which, in turn, makes up the liquid crystal display device for displaying an image on the liquid crystal panel. Note that, in reality, there are many other signal lines and other elements corresponding thereto, other than those shown in the drawing, which, however, are omitted here for convenience of explanation, and only eight signal lines f', f, a, b, c, d, e, e', and two scanning lines g_1 and g_2 are shown.

[0073]

The signal lines f', f, a, b make up a single block ("first block" hereinafter), and the signal lines c, d, e, e' make up another block ("second block" hereinafter). The following explanation of the present embodiment will be based on a structure of these two blocks, which, however, is not limiting.

[0074]

As shown in Fig. 1, to respective ends of the signal lines f', f, a, b, c, d, e, e' are provided signal line

switching elements (SWa, SWb, SWc, SWd, etc.), and the other ends of these switching elements are electrically connected to a signal line driving circuit (data transfer section) 1 as a signal input section for installing an external circuit, and between the signal line driving circuit 1 and the switching elements is provided a signal line branching section 7. The signal line switching elements may be realized by CMOS transistors, or, alternatively, NMOS transistors in some cases. The signal line branching section 7 can be structured by branching wires.

[0075]

The signal line switching elements are electrically and respectively connected to output lines s_1, s_2, s_3, s_4 which extend from output terminals of the signal line driving circuit 1. To control ends of the switching element SWa and other switching elements are connected, commonly to each of the plurality of blocks, control wires SW_1 and SW_2 for switching conduction/non-conduction of the signal line switching elements, and by this switching, an image signal (data signal) from the signal line driving circuit 1 is supplied in time division as a display signal to each signal line.

[0076]

That is, the signal lines or scanning lines are divided into blocks, and by dividing a period during which a scanning line is selected (one select period of a scanning line, one horizontal period) in the case of the signal line, or by dividing one vertical period in the case of the scanning line, the blocks to which the signal is destined are switched in time so that the data signal or scanning signal is sequentially applied to each block. In the present embodiment, the signal lines are divided into blocks, and the blocks to which the signal is destined are switched in time by dividing one select period of the scanning line so that the data signal is sequentially applied to each block. In the case of dividing the scanning lines into blocks, the blocks to which the signal is destined are switched in time by dividing one vertical period so that the scanning signal is sequentially applied to each block.

[0077]

The outputs of the control wires SW_1 and SW_2 are controlled by a conduction control section. Fig. 11 shows an exemplary structure of the conduction control section. Indicated by "HSY" is a horizontal synchronize signal which is synchronized with an image. A PLL (phase-locked

loop) oscillator 21 generates a clock CLK. The HSY and clock CLK are counted by an H counter (here, "H" indicates "Horizontal") 22, and a pulse is generated in decoders (SW_1 decoder 23, SW_2 decoder 24) based on the value of the counter. Each decoder is set to have a predetermined value in advance, and outputs a pulse based on this value. The predetermined value is decided and optimized beforehand with respect to individual parameters of the pixels or SWa, such as s_1 and g_1.

[0078]

Fig. 12 shows another structure example of the conduction control section. Here, instead of generating the clock CLK by the PLL oscillator 21 of Fig. 11, HSY and CLK are inputted to an H counter 31. The CLK is in synchronization with dot data of an image. The other structure is the same as that of Fig. 11.

[0079]

The following describes a structure of the signal line driving circuit 1. Fig. 18 shows one exemplary structure. Fig. 19 shows its timing chart. As shown in Fig. 18, from an input of a data line DAT to the output S_1 makes up a single sampling circuit (sampling section), and a total of n sampling circuits are provided. Note that, for convenience

of explanation, Fig. 18 only shows a first sampling circuit 71 and an nth sampling circuit 72, as representatives.

[0080]

The data line DAT is branched for input into n sampling circuits (sampling sections), and an image signal is outputted from each sampling circuit, via the output terminal (e.g., S_1), to a signal line. The data line DAT is for supplying the image signal, which is a data signal to be displayed on a pixel, to the signal line driving circuit 1. When the number of outputs of the data line DAT is n (n line outputs), and when the number of blocks is two as in the present example, the number of signal lines is given by their product, 2n. The image signal supplied from the data line DAT is sampled from the first (output terminal S_1) to the nth (output terminal S_n) signals at the timings of their respective sampling signals (sampling pulses) SAM_1 to SAM_n, which is then branched in the signal line branching section 7, so as to send the image signal to the 2n signal lines. The sampling signals SAM_1 to SAM_n may be created by shift resistors in the signal line driving circuit 1.

[0081]

To the data line DAT are connected analog switches

ASWA and ASWB as the first output. The data line DAT has a role of transferring an analog signal therein. The analog switches ASWA and ASWB are connected so as to transfer the image signal, which was inputted to the data line DAT, to an analog switch ASWD. Further, by the control of the analog switch ASWC, the input of the data line DAT is sent to the analog switch ASWD via either one of the analog switches ASWA and ASWB.

[0082]

Among two systems of inputs of the image signal as the data signal, the input which is transferred through the analog switches ASWC, ASWA, and ASWD will be referred to as a system A (indicated by "DA" in Fig. 18), and the input which is transferred through the analog switches ASWC, ASWB, and ASWD will be referred to as a system B (indicated by "DB" in Fig. 18). That is, the data line DAT has two parallel signal paths of system A and system B.

[0083]

Between the analog switch ASWA and the analog switch ASWD is disposed a sampling hold capacitor C_{SHA}. Similarly, between the analog switch ASWB and the analog switch ASWD is disposed a sampling hold capacitor C_{SHB}. Indicated by "RL" is a base potential.

[0084]

The analog switch ASWC receives the sampling signal SAM_1, and is switched under the control of a control signal CNT0.

[0085]

The analog switch ASWD outputs the image signal to an output buffer Bu, and is switched under the control of a control signal CNT. The output of the output buffer Bu makes up a first output terminal S_1.

[0086]

LEV is used to bring a charge level to a desired charge voltage in advance, as in the case of Fig. 4 (and Fig. 22 to be described later). That is, either a desired charge voltage is applied to the signal LEV, or the signal LEV is used as a switching timing signal so as to bring a voltage to a desired voltage, for example, by switching. This will be described later.

[0087]

The second and subsequent outputs are processed in the same manner as the foregoing first output.

[0088]

In order to drive the active-matrix substrate having the 2n signal lines, the following operations are carried

out. That is, the sampling signals (SAM_1 to SAM_n) from the shift resistors are sequentially supplied while a display signal which corresponds to a first block (data displayed on the left half of the screen) 11 of Fig. 3 is being supplied. Here, the control signal CNT0 selects the system A ("DA" in Fig. 18). Thus, the analog switch A (ASWA) is conducted, and the data signal of the first block is stored in the sampling hold capacitor (C_{SHA}).

[0089]

When the selection is finished up to SAM_n, the control signal CNT0 is switched to the system B ("DB" in Fig. 18), and the sampling signals (SAM_1 to SAM_n) are sequentially supplied again, and the image signals are supplied. Then, while the signal is being stored in the system B, the control signal CNT selects the system A so as to output the data signal which was stored previously.

[0090]

In the structure of Fig. 18, no data signal can be stored in the sampling hold capacitor of the system A or system B during a certain time period (in the vicinity of time t_5 in Fig. 19) in which the control signal CNT is switched from the system A to the system B. The image signal is generally supplied externally and continuously

per one horizontal line in a time sequential manner. Thus, in the structure of Fig. 18, when the time required for the sampling system to switch between the system A and the system B cannot be ignored with respect to a supply interval of the image signal, the data signal at the border of the first block and the second block is missed out in the display. To avoid this, a blanking period which corresponds to the time required for the switching is provided by making some modification to the image signal itself.

[0091]

Meanwhile, in the structures as shown in Fig. 5, Fig. 7, and Fig. 9, while sampling is made with the sampling signal SAM_1 continuously after the sampling signal SAM_1, unlike the structure of Fig. 18, they do not require a blanking period for latching or transfer. That is, because a single signal line driving circuit needs to be used twice or more in order to sample pixels of a single horizontal line (pixels of one horizontal line in the image display device), sampling is made with the sampling signal SAM_1 continuously and immediately after the sampling signal SAM_n. The structure of Fig. 18, to this end, requires a time interval between SAM_n and SAM_1 since it requires

time for the transfer, etc. of the data signal. In contrast, in the structures of Fig. 5, Fig. 7, and Fig. 9, the continuous sampling is made possible by having different group control signals for the front half and the rear half of the number of outputs, without taking a special measure, such as modification to the image signal itself, to provide a blanking period.

[0092]

The following explains an exemplary structure as shown in Fig. 5. The structure of Fig. 5 differs from that of Fig. 18 by the arrangement of signals for controlling sampling. Note that, for convenience of explanation, Fig. 5 only shows a first sampling circuit 15 and an nth sampling circuit 16 as representative sampling circuits.

[0093]

When the number of outputs is n (n line outputs) as in the foregoing case, in the structure of Fig. 5, unlike that of Fig. 18, the outputs are grouped into a first group which includes the first output (S_1) to the (n/2)th output ($S_{n/2}$), and a second group which includes the (n/2+1)th output ($S_{n/2+1}$) to the nth output (S_n). Here, n is an even number. From the first output (S_1) to the (n/2)th output ($S_{n/2}$), the analog switch ASWC is controlled by a group

control signal CNTa for the lines of the front half, and from the (n/2+1)th output ($S_{n/2+1}$) to the nth output (S_n), the analog switch ASWC is controlled by a group control signal CNTb for the lines of the rear half. That is, there are two kinds of group control signals, CNTa and CNTb, for switching the sampling signals SAM_1 to SAM_n between the system A and the system B. The switching by the group control signals CNTa and CNTb is made in the vicinity of $SAM_{n/2}$. This is because SAM_1 is sampled continuously and immediately after the sampling of SAM_1 to SAM_n is finished, and to eliminate the need for specially modifying the data signal supplied to the data line. Note that, the other structure is the same as that of Fig. 18.

[0094]

Fig. 6 shows a timing chart. In Fig. 6, the systems which are selected by the group control signals CNTa and CNTb and the control signal CNT are indicated in brackets. That is, the period in which the system A is selected is indicated by (DA) and the period in which the system B is selected is indicated by (DB). Also, as to LEV, its output level is fixed during a high period in Fig. 6, and its effect is the same as the case of Fig. 18.

[0095]

In this manner, in this structure, unlike that of Fig. 18, the sampling signals are divided into two groups. That is, n sampling circuits (sampling sections) are connected by dividing them in half, corresponding to the group control signals CNTa and CNTb, respectively. The data signals of a half (n/2) of the first block 11 (see Fig. 3) are stored in the C_{SHA} at the timings of SAM_1 to $SAM_{n/2}$ by the selection of the system A by the group control signal CNTa, which is the control signal for controlling these data signals. The remaining n/2 data signals are stored in the C_{SHA} of their corresponding sampling circuits at the timings of $SAM_{n/2+1}$ to SAM_n, wherein the system A has been selected in advance by the group control signal CNTb, which is the control signal for selecting these data signals, at the timing of $SAM_{n/2+1}$. Even when the selection is made in advance in this manner, no adverse effect is caused during a non-select period of $SAM_{n/2+1}$ to SAM_n.

[0096]

When the selection of $SAM_{n/2+1}$ to SAM_n is started, the group control signal CNTa selects the system B, thus getting ready to hold the in-coming image signals of the second block (data which correspond to the right half of the screen) 12. Evidently, during a selection period of

$SAM_{n/2+1}$ to SAM_n, the first to (n/2)th sampling circuits are in a stand-by state, and no sampling is actually carried out therein. After the selection is finished up to SAM_n, the sampling signals (SAM_1 to SAM_n) are sequentially supplied again, and the image signals are supplied. Then, the control signal CNT selects the system A while signals are being stored in the system B, so as to output the data signal which was stored previously. This structure allows sampling of the next block SAM_1 immediately after the sampling up to SAM_n is finished. As a result, the image signals of the first block and the image signals of the second block are continuously transmitted, allowing the data signals (image signals) to be admitted without causing any problem, even when the data signals of the second block are continuously sent immediately after the sampling of the first block up to SAM_n is finished.

[0097]

The following describes an exemplary structure as shown in Fig. 7. The structure of Fig. 7 differs from those shown in Fig. 5 and Fig. 18 by the structure of the sampling circuit. For convenience of explanation, Fig. 7 only shows a first sampling circuit 17 and an nth

sampling circuit 18 as representative sampling circuits. Indicated by "ASWS" is an analog switch for sampling. "ASWH" is an analog switch for holding. "C_s" is a sampling capacitor and "C_H" is a holding capacitor.

[0098]

Grouping is as shown in Fig. 5. That is, when the number of outputs is n (n line outputs) as in the foregoing case, unlike Fig. 18, the outputs are grouped into the first group which includes the first output (S_1) to the (n/2)th output ($S_{n/2}$), and the second group which includes the (n/2+1)th output ($S_{n/2+1}$) to the nth output (S_n). Here, n is an even number. From the first output (S_1) to the (n/2)th output ($S_{n/2}$), the analog switch ASWH is controlled by the group control signal CNTa which is used for the lines of the front half, and from the (n/2+1)th output ($S_{n/2+1}$) to the nth output (S_n), the analog switch ASWH is controlled by the group control signal CNTb which is used for the lines of the rear half. That is, there are two kinds of group control signals, CNTa and CNTb, for controlling sampling of the sampling signals SAM_1 to SAM_n. The transfer in the first group is made in the vicinity of $SAM_{n/2}$. This is because SAM_1 is sampled continuously and immediately after the sampling of SAM_1 to SAM_n is finished, and to

eliminate the need for specially modifying the data signals supplied to the data lines. The other operations are the same as those described in Fig. 18.

[0099]

Fig. 8 shows a timing chart. In Fig. 8, the transfer periods of image signals by the group control signals CNTa and CNTb are indicated by T_{21} and T_{22}, respectively. The output level of LEV is fixed during a period T_{23}, and its effect is as described in Fig. 18.

[0100]

In this manner, in this structure, unlike that of Fig. 18, the sampling signals are divided into two groups. That is, n sampling circuits (sampling section) are connected by dividing them in half, corresponding to the group control signals CNTa and CNTb, respectively. The data signals of a half (n/2) of the first block 11 (see Fig. 3) are stored in the C_H of their respective sampling circuits at the timings of SAM_1 to $SAM_{n/2}$. The remaining n/2 data signals are stored in the C_H of their corresponding sampling circuits at the timings of $SAM_{n/2+1}$ to SAM_n.

[0101]

When $SAM_{n/2+1}$ to SAM_n are selected and storing of their data signals is started, the data signals of SAM_1 to

$SAM_{n/2}$, which are stored in C_H, are transferred (period T_{21}) by the group control signal CNTa, which is the control signal, thus getting ready to hold the in-coming image signals of the second block (data which correspond to the right half of the screen). Evidently, during a selection period of $SAM_{n/2+1}$ to SAM_n, the first to (n/2)th sampling circuits are in a stand-by state, and no sampling is actually carried out therein. After the selection is finished up to SAM_n, the sampling signals (SAM_1 to SAM_n) are sequentially supplied again, and the image signals are supplied. When SAM_1 to $SAM_{n/2}$ is selected and storing of their data signals is started, the data signals of $SAM_{n/2+1}$ to SAM_n, which are stored in C_H, are transferred (period T_{22}) by the group control signal CNTb, which is the control signal. This structure allows sampling of the next block from SAM_1 immediately after the sampling up to SAM_n is finished.

[0102]

As described, the structure of Fig. 7 includes, instead of the two sampling systems of Fig. 5 and Fig. 18 which are provided in parallel for each output, two serial capacitors, which allows output and admission of the signals at the same time by transferring the signals for

each admission. In the structure of Fig. 18, there is only one control signal for holding and transfer (control signal CNT0). In contrast, in the example of Fig. 7, as in Fig. 5, the control signal is divided into two (group control signals CNTa and CNTb). In the admission of signals in the first block, while the sampling signal $SAM_{n/2+1}$ to SAM_n are being selected, the data signals of SAM_1 to $SAM_{n/2}$ are transferred to be ready for holding the in-coming image signals of the second block. As a result, the image signals of the first block and the image signals of the second block are continuously transmitted, thus admitting data signals (image signals) without causing any problem, even when the data signals of the second block are sent continuously and immediately after the sampling of the signals of the first block up to SAM_n is finished.

[0103]

The following describes an exemplary structure as shown in Fig. 9. Fig. 9 shows the case of digital data of m bits. For convenience of explanation, Fig. 9 only shows a first sampling circuit 19 and an nth sampling circuit 20 as representative sampling circuits. The data line DAT has the function of transferring a digital signal. The number of tones is m bits. In Fig. 9, an image signal inputted from

the terminal on the left end is branched and sequentially inputted to m data lines DAT, i.e., data lines of m bits, and, respectively, to two D-type flip-flops and an D/A convertor DAC, to be outputted as image signals (S_1, S_2, ... S_n).

[0104]

Grouping is as shown in Fig. 5 and Fig. 7. That is, when the number of outputs is n (n line outputs) as in the foregoing case, unlike Fig. 18, the outputs are grouped into the first group which includes the first output (S_1) to the (n/2)th output ($S_{n/2}$), and the second group which includes the (n/2+1)th output ($S_{n/2+1}$) to the nth output (S_n). Here, n is an even number. From the first output (S_1) to the (n/2)th output ($S_{n/2}$) are controlled by a group controlling signal LSa for controlling a latch for the lines of the front half, and, from the (n/2+1)th output ($S_{n/2+1}$) to the nth output (S_n) are controlled by a group controlling signal LSb for controlling a latch for the lines of the front half. That is, there are two kinds of group control signals, LSa and LSb, for controlling sampling of the sampling signals SAM_1 to SAM_n. The transfer of the first group is carried out in the vicinity of the $SAM_{n/2}$. This is because SAM_1 is sampled continuously and immediately after the

sampling of SAM_1 to SAM_n is finished, and to eliminate the need for specially modifying the data signals supplied to the data lines. The other operations are the same as those described in Fig. 18.

[0105]

Fig. 10 shows a timing chart. In Fig. 10, the transfer periods of image signals by the group control signals LSa and LSb are indicated by t_{31} and t_{32}, respectively. The output level of LEV is fixed during a period t_{33}, and its effect is as described in Fig. 18.

[0106]

In this manner, in this structure, unlike that of Fig. 18, the sampling signals are divided into two groups. That is, n sampling circuits (sampling section) are connected by dividing them in half, corresponding to the group control signals LSa and LSb, respectively. The data signals of a half (n/2) of the first block 11 (see Fig. 3) are stored in the two D-type flip-flops of their corresponding sampling circuits at the timings of SAM_1 to $SAM_{n/2}$. The remaining n/2 data signals are stored in the two D-type flip-flops of their corresponding sampling circuits at the timings of $SAM_{n/2+1}$ to SAM_n.

[0107]

When $SAM_{n/2+1}$ to SAM_n is selected and storing of their data signals is started, the data signals SAM_1 to $SAM_{n/2}$, which are stored in the two D-type flip-flops, are transferred (time t_{31}) by the group control signal LSa, which is the control signal, thus getting ready to hold the in-coming image signals of the second block (data which correspond to the right half of the screen) 12. Evidently, during a selection period of $SAM_{n/2+1}$ to SAM_n, the first to (n/2)th sampling circuits are in a stand-by state, and no sampling is actually carried out therein. After the selection is finished up to SAM_n, the sampling signals (SAM_1 to SAM_n) are successively supplied again, and the image signals are supplied. When SAM_1 to $SAM_{n/2}$ are selected and storing of their data signals is started, the data signals $SAM_{n/2+1}$ to SAM_n, which are stored in the two D-type flip-flops, are transferred (time t_{32}) by the group control signal LSb, which is the control signal. This structure allows sampling of the next block from SAM_1 immediately after the sampling up to SAM_n is finished.

[0108]

As described, the structure of Fig. 9 includes, instead of the two sampling systems of Fig. 5 and Fig. 18 which are provided in parallel for each output, two serial

D-type flip-flops, which allows output and admission of the signals at the same time by transferring the signals for each admission. In the structure of Fig. 18, there is only one control signal for holding and transfer (control signal CNT0). In contrast, in the example of Fig. 9, as in Fig. 5 and Fig. 7, the control signal is divided into two (group control signals LSa and LSb). In the admission of signals in the first block, while the sampling signal $SAM_{n/2+1}$ to SAM_n are being selected, the data signals of SAM_1 to $SAM_{n/2}$ are transferred to be ready for holding the in-coming image signals of the second block. As a result, the image signals of the first block 11 and the image signals of the second block 12 are continuously transmitted, thus admitting data signals (image signals) without causing any problem, even when the data signals of the second block are sent continuously and immediately after the sampling of the signals of the first block up to SAM_n is finished.

[0109]

Fig. 13 shows an exemplary structure of a generating section of the control signal CNT and the group control signals CNTa and CNTb. Indicated by "VSY" is a vertical synchronize signal which is synchronized with an image.

The input signals to an H counter 41 are the same as those in the examples of Fig. 11 and Fig. 12. A pulse of one horizontal period is inputted from the H counter 41 to a V counter 42 (here, "V" indicates "vertical"). The HSY (and clock CLK) is counted in the H counter 41 and the V counter 42, and decoders (CNT decoder 43, CNTa decoder 44, and CNTb decoder 45) respectively generate pulses based on the values of the counters. Note that, the control signal CNT0 can also be generated in the same manner as the group control signals CNTa and CNTb, by designating one of the CNTa decoder 44 and the CNTb decoder 45 as a CNT0 generating decoder and by omitting the other in the arrangement of Fig. 13. Each decoder outputs, as in the examples of Fig. 11 and Fig. 12, a pulse according to a predetermined value which has been set beforehand. The predetermined value varies depending on the number of outputs of drivers, etc., and is decided and optimized beforehand based on these factors. Note that, an arrangement wherein a PLL oscillator is provided may also be adopted as in Fig. 11.

[0110]

In Fig. 13, each decoder comes into operation, taking into consideration an output of the V counter 42. This is

because, while a pulse which periodically changes at the same timing in one horizontal period can be created by the use of the H counter alone as in the case of Fig. 11 and Fig. 12, the control signal CNT, etc., does not show the periodic change at the same timing in one horizontal period, which necessitates using the V counter (by which counting is made per one horizontal period).

[0111]

Fig. 14 through Fig. 17 show exemplary structures of an output buffer Bu. Fig. 14 shows the case where a desired charge voltage is added to a signal LEV in the structure of Fig. 18. Fig. 15 shows the case where switching is made to a desired charge voltage Vd using the signal LEV as a timing signal in the structure of Fig. 18. Note that, in Fig. 14 and Fig. 15, "ASWD" applies to the case of Fig. 5 and Fig. 18, and "ASWD" becomes "ASWH" in the case of Fig. 7. A signal from the ASWD is inputted to an OP amplifier (operational amplifier) 51. In Fig. 14, the LEV is inputted directly as a charge voltage to a switch 52, and also as a signal which indicates a switching timing via a level shifter 53 to the switch 52. In Fig. 15, the LEV is inputted as a signal which indicates a switching timing directly to the switch 52, and a desired charge voltage Vd

is inputted to the switch 52.

[0112]

Fig. 16 and Fig. 17 show exemplary structures of the D/A (digital/analog) convertor DAC. Fig. 16 shows the case where a predetermined charge voltage is added to the signal LEV in the structure of Fig. 9. Fig. 17 shows the case where switching is made to a predetermined charge voltage Vd with the use of the signal LEV as a timing signal in the structure of Fig. 9. In each of n sampling circuits of Fig. 9, a signal DFF immediately before the DAC, i.e., a signal from the output Q of the D-type flip-flop of the second stage, is inputted to the D/A convertor 61. In Fig. 16, the LEV is inputted directly as a charge voltage to the switch 62, and as a signal which indicates a switching timing via the level shifter 63 into the switch 62. In Fig. 17, the LEV is directly inputted as a signal which indicates a switching timing into the switch 62, and a predetermined charge voltage Vd is inputted to the switch 62.

[0113]

The foregoing operation can be realized relatively easily by making up the structure using the switch. Even though the predetermined charge voltage Vd can

alternatively be inputted externally from the source driver (signal line driving circuit 1), the inconvenience of supplying power externally from the driver can be eliminated by directly providing operation power for the source driver, or by using a voltage which is resistively divided from the operation power.

[0114]

Note that, in any of the foregoing structures of Fig. 5, Fig. 7, and Fig. 9, it is not necessarily required for the sampling circuits to be grouped exactly in half, as long as they are grouped into a plurality of groups. Further, the number of groups is not just limited to two. More specifically, the sampling circuits are grouped into a predetermined number of groups based on a switching time which is decided by a clock frequency and a switching rate of each analog switch (ASWA, etc.). The border of grouping in this example is at n/2 since this provides the widest margin.

[0115]

The following will describe a data transfer operation and a state of image signals by the foregoing structures. Note that, the explanation will be given through the case of a display screen with vertical stripes of three tones as

shown in Fig. 3, instead of a display screen of entire black.

[0116]

To explain its basic operation, while a certain scanning line g_1 is being selected (see Fig. 1), i.e., while a certain line is selected, a pulse (signal line switching element control signal) is sent from each decoder as shown in Fig. 11 and Fig. 12 subsequently to the control wires SW_1 and SW_2, so as to conduct the signal line switching elements (e.g., SWa). Then, by the selection of SW_1, the signal line switching elements SWa and SWb are conducted. As a result, image signals from the signal line driving circuit 1 are supplied to the signal lines a and b. Because the scanning line g_1 is selected, the image signals of the signal lines a and b are applied to pixels A_1 and B_2, respectively. Here, since SW_2 is non-selected, no image signals are supplied to signal lines c and d. Thereafter, SW_1 become non-selected, and SWa and SWb become non-conducted, thus holding the signal lines a and b and the pixels A_1 and B_1. Then, when SW_2 is selected and the signal line switching elements SWc and SWd are conducted, image signals from the signal line driving circuit 1 are supplied to the signal lines c and d, and

since the scanning line g_1 is selected, the image signals of the signal lines c and d are applied to the pixels C_1 and D_1, respectively.

[0117]

The scanning lines g_1 and g_2 are supplied by the scanning line driving circuit 2, as shown in Fig. 3, and image signals are supplied from the signal line driving circuit 1 so that the vertical stripes becomes thinner in the display areas 3, 4, and 5 in this order. Fig. 2 shows a state of image signals under this condition. In the present embodiment, prior to the timings (t_3 and t_4 in Fig. 2) of supplying normal image signals (data signals) to the signal lines by the normal selection of the control wires, selection is made at t_1 and t_2 as shown in Fig. 2 to invert the polarity of the signal lines in advance. The selection of the control wires SW_1 and SW_2 is distinguished between normal selection and preliminary selection, where the former refers to selection which is normally carried out, and the latter refers to selection which is carried out prior to the normal selection. In the present embodiment, while a single line is being selected by switching on the scanning line (select period, one horizontal period), the signal lines c, d, e, e' which belong to the second block 12

are preliminarily conducted prior to the end of a period in which the image signal is normally applied to each line (each lines of scanning signals g_1 and g_2, etc.) as normal conduction of the first block 11 (signal lines f', f, a, b), so as to invert the polarity. At the timing t_2 at which SW_2 is selected, the signal line b has a hike as in the conventional structure shown in Fig. 32. However, the normal timing of the image signal is t_3, and a correct potential is given by the application to the signal line via the signal line switching element, and this state is maintained until the scanning line g_1 becomes non-selected. As a result, the foregoing problem of visible border can be solved.

[0118]

In the driving method of Fig. 2, as shown therein, the image signal is divided according to intervals T_1 and T_2 in a chronological order within one select period of the scanning line, and image signals which are supplied in a time sequential manner are sent sequentially to the signal lines from the signal line driving circuit 1 in such a manner that the image signals of the first block are first admitted by the multiplexer of the signal line driving circuit 1 in interval T_1, and then the image signals of the

second block are admitted in interval T_2.

[0119]

Incidentally, as the timing t_4, the potential given to the signal line c is different from that given at t_2, and there are cases where the signal line b is hiked according to the potential difference. However, the potential difference is sufficiently small compared with the polarity inversion of the image signal, and, in many cases, it does not become visible. However, in case where oscillation of the signal line b due to the potential difference becomes visible by the magnitude of the parasitic capacitance Csd, it is effective to apply the image signal as shown in Fig. 4. The following explains how this is done.

[0120]

A desired voltage is applied at the time of preliminary polarity inversion, separately from the output signal (image signal) from the signal line driving circuit 1. In the signal driving system according to Fig. 4, the signal line driving circuit 1 has incorporated a memory function for storing such a desired voltage. Specifically, the signal LEV as shown in Fig. 5, Fig. 7, and Fig. 9 is used. That is, as noted above, a desired charge voltage is added to the signal LEV. In this case, the desired charge voltage added

to the signal LEV has signal intensity which has been increased or decreased from the value of signal intensity at the time of the normal polarity inversion of the first block 11, so as to have a value close to the signal intensity at the time of the normal polarity inversion of the second block 12. Further, here, the signal supplied as the desired charge voltage to the signal LEV has the same potential as that applied at the time of the normal potential inversion of the second block 12 in which the preliminary polarity inversion is carried out.

[0121]

Alternatively, as noted above, the voltage may be, for example, switched to the desired voltage (Vd) in accordance with the input timing of the signal LEV.

[0122]

In this manner, the image signals which correspond to the first block 11 and the second black 12, respectively, are also supplied in the described manner to the output lines s_1 through s_4 at the timings of t_1 and t_2, and the signals are accurately applied to the signal lines and the pixels at the timings t_3 and t_4 after raising the signal lines roughly to a predetermined voltage. Here, the term "roughly" indicates a degree which does not cause

oscillation on the signal line at the border at the time of t_3 and t_4, and it is not necessarily required to have a potential exactly the same as that of the output lines s_1 through s_4. That is, the select period (data signal is applied) of the signal lines selected at the timings t_1 and t_2 can be made short to some extent.

[0123]

Further, depending on restrictions of time for the admission of the signals in the signal line driving circuit 1, the image signals of a previous line or previous frame may be supplied at the timings t_1 and t_2 by suitably setting their polarity. In this way, substantially the same effect can be obtained.

[0124]

In the structure as shown in Fig. 18, the CNT selects the system B and a display signal of interval T_2 is outputted while the system A is selected by the CNT0 and the display signal is being admitted in the sampling hold capacitors C_{SHA} and C_{SHB}. This structure is limited to the case where the data signals which are supplied in a time sequential manner are outputted without resulting in change in order, and in order to carry out the driving as shown in Fig. 4, since the data signals cannot be inputted

and outputted simultaneously, it is required to quickly receive the two systems of data signals and output them at their respective timings, or to increase the capacity of the sampling hold capacitors (C_{SHA} and C_{SHB}) in parallel, or to have a memory function on the supply side of the data signals.

[0125]

Incidentally, in the structure of Fig. 18, the CNT0 selects the system B at the timing t_5 (see Fig. 19), and starts to admit a new data signal. By inverting the polarity in advance, the signals of the system B of the previous line are supplied with the same polarity prior to the selection at t_3 and t_4. Evidently, it is required here that the signals of the scanning lines of the previous stage have been switched off beforehand. Further, in the case of driving with a plurality of blocks, it is required to increase the number of sampling hold capacitors in parallel, or to add a memory function on the side of supplying the data signals.

[0126]

There is high probability that the display signal of the previous line has the same display state as the display signal of the current line, and even at the border where

the display in the vertical direction changes, the voltage oscillation is significantly smaller compared with the conventional example where signals are applied with the opposite polarity, and therefore the foregoing display deficiency is limited to one pixel, and the possibility of this deficiency becoming visible is very small.

[0127]

When the signal line driving circuit 1 has a line memory with the memory function, the display signals of the previous frame can be supplied only by setting their polarity. In this case, the foregoing display deficiency appears only at the moment when the display state changes from the previous frame, and the border of the blocks does not become visible.

[0128]

Note that, the same hike also occurs at the moment when the destination of the image signals is changed from the second block to the first block, when SW_1 is selected while SW_2 is non-selected; however, no display problem is caused on pixel C_1 because the potential is replaced with a correct potential by the selection of SW_2 at the next timing while the scanning line g_1 is being selected. Further, the oscillation of the scanning line g_1 due to C_{sd} during

non-conduction thereof varies depending on the signal line which is capacitively coupled with the pixels, but the difference is insignificant as the effective value of the entire display period and no problem is caused.

[0129]

The present embodiment thus prevents degradation of display quality due to potential oscillation of the signal lines. Note that, the present embodiment explained the case where two blocks are provided, but it is also applicable to driving employing a larger number of blocks.

[0130]

In the present embodiment, in the case of two blocks, as shown in Fig. 2, among the two ON (High) periods of the control wire SW_1 in one select period of the scanning line, the one which starts with time t_1, which is the preliminary polarity inversion period, has ON time a_1 and OFF time b_1, and the one which starts with time t_3, which is the normal polarity inverse period, has ON time c_1 and OFF time d_1. Similarly, among the two ON (High) periods of the control wire SW_2 in the select period of the scanning line, the one which starts with time t_2 has ON time a_2 and OFF time b_2, and the one which starts with time t_4 has ON time c_2 and OFF time d_2. Here, $b_2 \leq d_1$. Also, $b_1 \leq a_2$, and

$d_1 \leq c_2$. Further, $b_2 \leq c_1$.

[0131]

In the same manner, it is assumed here that there are N blocks (where N is an integer of not less than 2), where the blocks are adjacent to each other in order from the first to the Nth blocks. Fig. 20 shows an example where the number of blocks N is 4. That is, four control wires SW_1, SW_2, SW_3, SW_4 are used. Here, with respect to a kth block where k is an integer of not less than 2 and not more than N, among the two ON (High) periods of the control wire SW_k in one select period of the scanning line, the one which is the preliminary polarity inversion period has ON time a_k and OFF time b_k, and the one which is the normal polarity inverse period has ON time c_k and OFF time d_k. Here, when $d_{k-1} \leq c_k$, i.e., when the normal polarity inverse time (time at which a normal data signal is applied) is delayed as the number increases, the relation $b_k \leq d_{k-1}$ is set. Also, $b_{k-1} \leq a_k$ is set. That is, the start time of the preliminary polarity inversion is delayed as the number increases so that it is after the end time of the preliminary inversion of the previous block. Note that, alternatively, $b_k \leq a_{k-1}$ may be set. That is, the end time of the polarity inversion may be advanced as the number

increases so that it is before the start time of the polarity inversion of the previous block. Further, in either case, the preliminary polarity inverse periods of arbitrary adjacent blocks may have an overlap time.

[0132]

Further, it is also possible to have a relation $b_N \leq c_1$. That is, the end time of the preliminary inverse period of an Nth block may be on or before the start time of the normal inverse period of the first block, which, however, is not limiting. However, the end time of the preliminary polarity inversion of the last block N is preferably before the start time of the normal polarity inversion (data signal is applied) of the first block for the following reasons. When the signal line switching elements (e.g., SWa) of a certain block is ON while another block is supplying a normal data signal, there will be an increase in load on various places of the signal line driving circuit 1 and panel (liquid crystal panel), e.g., auxiliary capacitor wiring (not shown), and due to the influence of signal delay, etc., the charge characteristics of the block to which the normal data signal is supplied may become different from that of other blocks. This may not cause any problem depending on driving capacity of the signal line driving

circuit 1, a load or size of the panel, a pre-set charging rate, i.e., a resistance value of the pixel transistor or signal line switching element. Note that, such a structure is shown in Fig. 24 to be described later.

[0133]

Further, as shown in Fig. 3, when the block to which the data signal is applied by the conduction of the control wire SW_1 is on the left end of the screen (first block 11), i.e., when it is the first block to which the normal data signal is applied, the preliminary polarity inversion (polarity inversion at t_1) is not required. However, since it is preferable in actual practice to exactly match the charging rate, etc., among blocks, it is preferable to have the same release time or waveform (conduction timing, etc.) for the control wires SW_1, SW_2, ... This also applies to the following embodiments.

[0134]

(Second Embodiment)

The following will describe another embodiment of the present invention referring to Fig. 21 and Fig. 22. Note that, for convenience of explanation, elements having the same functions as those explained in the drawings of the foregoing embodiment are given the same reference

numerals and explanations thereof are omitted here.

[0135]

In the present embodiment, as shown in Fig. 21, a plurality of blocks are selected once at the same time prior to the selection of each block, so as to invert the polarity of signal lines. Fig. 21 only show two blocks and their effect appears nominal. In reality, however, in the case of driving using many blocks, for example, four blocks, it becomes important to select the blocks simultaneously and to end the polarity inversion of the signal lines in a short period of time, in order to secure enough time for supplying an accurate potential to each block in the subsequent operation. The duration of the periods which are selected simultaneously is set such that the signal line at the border is not affected by oscillation, and, specifically, it is sufficient to have a value twice the time constant which is given by the signal line switching element and the signal line capacitance.

[0136]

In this manner, in the present embodiment, under the restriction where the driving is made per block, the signals are supplied simultaneously prior to sequentially supplying image signals to the respective signal lines, so

as to apply inverse signals in advance to prevent the border of the blocks from becoming visible. This reduces display deficiency due to potential fluctuation by C_{sd}.

[0137]

Incidentally, it was mentioned that the signal line b experiences a slight hike by the change in potential of the signal line c at the timing t_4. This slight potential fluctuation becomes most visible when displaying half-tones. To say it backwards, no deficiencies due to t_4 will be caused by the setting which eliminates the deficiencies in half-tones. Even though the image signal applied to the first block is given at t_1 in Fig. 21, as shown in Fig. 22, by supplying a half-tone image signal at t_1, there will be no fluctuation at the timing t_4 when a half-tone is displayed on the lines which correspond to the signal lines b and c. The half-tone image signal used here is prepared as the signal LEV as discussed above. That is, the LEV is used to bring a charge level to a desired charge voltage in advance, as explained in the First Embodiment with reference to Fig. 4. Namely, either a desired charge voltage is applied to the signal LEV, or the signal LEV is used to bring a voltage to a desired voltage, for example, by switching.

[0138]

The largest potential fluctuation occurs when a half-tone voltage is applied to the signal lines b and c at t_1 and when a black or white voltage is supplied to the signal line c at t_4. Even in this case, while the signal line b is at the black or white potential at t_3, no abnormality on pixel B_1 is recognized because a change in transmittance of the liquid crystal with respect to the potential fluctuation is small, and since the pixel B_1 is on the border at which the tone of adjacent pixels changes, the potential fluctuation does not become visible even when the signal b remains at the half-tone at t_3.

[0139]

The definition as discussed in the First Embodiment can be applied as follows in the present embodiment. When the number of blocks is two, the relation of $b_2 \leq d_1$ is set. Also, $a_1 = a_2$, $b_1 = b_2$, and $d_1 \leq c_2$. Further, $b_2 \leq c_1$.

[0140]

Similarly, in the case of N blocks, $b_k \leq d_{k-1}$, and $a_1 = a_2 = \ldots = a_N$, $b_1 = b_2 = \ldots = b_N$, and $d_{k-1} \leq c_k$. Further, as in the First Embodiment, $b_N \leq c_1$.

[0141]

(Third Embodiment)

The following will describe yet another embodiment of the present invention referring to Fig. 23 and Fig. 24. Note that, elements having the same functions as those described in the drawings of the foregoing embodiments are given the same reference numerals and explanations thereof are omitted here.

[0142]

In the present embodiment, unlike the First and Second Embodiments, SW_2 is selected purposefully before SW_1 is switched to non-select. Fig. 23 shows how this is done. At the time when the polarity of the signal line c is inverted at t_4, the signal line switching element SW_1 of the signal line b is still being conducted, and therefore s_4 is in accordance with the supplied voltage, and, unlike the conventional case, s_4 is not fixed by the application of the signal to the pixel while there is a hike. Because it is not required to provide a period for conducting SW_2 as in the First and Second Embodiments, it is possible to increase the time for applying a normal voltage via the signal line switching element (voltage applied at the time of normal polarity inversion). The electrostatic capacitance of the signal lines is generally large, and thus it is difficult to lower the resistance value of the switching elements to the

extent which allows a signal with a sufficiently small time constant. The driving method of the present embodiment is very useful in such a case.

[0143]

Further, since it is not required to generate a pulse, etc., which is discrete to the preliminary polarity inversion, the signal waveform of the control wire can be made simpler. As a result, a circuit for generating signals for the control of the signal line driving can be made simpler.

[0144]

Here, depending on the performance of the signal line driving circuit or impedance of wiring on the active-matrix substrate, there are cases where the potential of the image signals of the output lines s_1 through s_4 falls at t_4 in Fig. 23. This is caused by an abrupt increase in voltage, and the potential returns to a desired potential after a certain elapsed time. However, since t_4 is immediately before the time when SW_1 becomes non-selected, there are cases where the instantaneous voltage drop affects the last stage of signal application to the pixels, and as a result the voltage is fixed at the dropped level. The following describes this.

[0145]

In order to prevent this, in Fig. 24, the polarity of the signal line c is inverted by selecting SW_2 at the early stage of the SW_1 selection. Then, SW_2 is non-conducted to accurately supply image signals to the signal lines f, a, and b, and SW_2 is conducted again after SW_1 becomes non-conducted, so as to accurately supply image signals to the signal lines c, d, and e. Here, particularly, the preliminary conduction start time of SW_2 is set to coincide with the normal conduction start time of SW_1.

[0146]

The time for applying a signal to the normal voltage via the signal line switching element can also be increased by this method, and the same effects as that described in Fig. 1 and Fig. 21 can be obtained as to the problem of visible border. Further, unlike the method of Fig. 23, the foregoing method provides enough time from the end of preliminary conduction of SW_2 to the end of normal conduction of SW_1, thus effectively preventing the voltage drop and obtaining desirable charge characteristics.

[0147]

In the case of multiple-block driving, instead of two-block driving, a period of selecting a previous block (polarity inverse period), by design, partially overlaps a

period of selecting the subsequent block in the driving method of Fig. 23, and the period of selecting a previous block is preferably set to overlap the period of selecting the subsequent block also in Fig. 24, as in the foregoing case. For example, in Fig. 24, a pulse (high period) of SW_1 starting with $time_{t11}$ overlaps a pulse (high period) of SW_2 starting with t_{12}. This is due to the fact that the display state tends to be relatively similar between adjacent blocks and thus, in many cases, the voltage which has been subjected to polarity inversion is the same as the normally applied voltage, and therefore the influence of oscillation due to signal application to the subsequent block after the previous block became non-conducted tends to become less.

[0148]

As described, the example as shown in Fig. 23 has a structure wherein the normal polarity inverse periods have an overlap time with respect to two blocks in which the times of applying the data signals are in succession. Another way of saying this, by defining the polarity inversion in terms of the normal polarity inversion and the preliminary polarity inversion as explained in the First Embodiment (see Fig. 2, Fig. 21, Fig. 24), is that the

preliminary polarity inversion of a subsequent block (second block) is finished at the time when the normal polarity inversion of a certain block (first block) is finished, and continuously thereafter the normal polarity inversion of the second block is started.

[0149]

Further, in the example of Fig. 24, the preliminary polarity inversion of the subsequent block (second block) is carried out in the vicinity of the time the normal polarity inversion of a certain block (first block) is started. Alternatively, the structure of Fig. 24 may be modified to have a structure wherein the start time of the preliminary polarity inversion of the second block is before the start time of the normal polarity inversion of the first block, or the end time of the preliminary polarity inversion of the second block is also before the start time of the normal polarity inversion of the first block. It is also possible to have an intermediate structure wherein, in Fig. 24, the start time of the preliminary polarity inversion of the second block is before the start time of the normal polarity inversion of the first block, and the end time of the preliminary polarity inversion of the second block is before the end time of the normal polarity inversion of the

first block.

[0150]

In each of the foregoing embodiments, in the case where the active-matrix substrate is used for a color display device, it is preferable that the correspondence of pixels with respect to the output terminals of the signal line driving circuit does not differ in color among blocks. This means that, for example, when pixel A_1 receives an image signal from the output line s_3 in the first block and pixel E_1 (not shown) receives the image signal from the output line s_3 in the second block in the two-block driving, both pixel A_1 and pixel E_1 display red (R). This is to increase, in the polarity inversion prior to the application of the normal image signal, the probability of having the same voltage as the normal apply voltage of the subsequent block when supplying a voltage of the line to the signal line. For example, in the case of displaying a monochromatic half-tone on the entire screen, since the border becomes highly visible in the conventional driving, there is strong need for effectively utilizing the structures of the present invention, and it is important not to have different colors among blocks.

[0151]

The foregoing embodiments described the display device incorporating pixels, which uses the active-matrix substrate employing the data transfer method of the present invention, and, in particular, the liquid crystal display device which uses liquid crystal for the pixels. However, not limiting to this, the present invention is also applicable, for example, to detectors, for example, such as an X-ray sensor, which use the photoelectric effect.

[0152]

(Fourth Embodiment)

The following will describe still another embodiment of the present invention referring to Fig. 25. Note that, elements having the same functions as those described in the drawings of the previous embodiments are given the same reference numerals and explanations thereof are omitted here.

[0153]

The preset embodiment is a photodetector, such as an X-ray sensor, which employs the photoelectric effect. As shown in Fig. 25, a photodetector panel 102, a signal processing section (data transfer section) 101, and a data storage unit 110 are connected in this order.

[0154]

Inside the photodetector panel 102 are provided signal lines S_k (k = 1, 2, ... N) and scanning lines (not shown) which are formed in a matrix pattern as in the First Embodiment, and the signal lines are branched into a plurality of blocks (not shown) as in the First Embodiment. Where the pixels were provided in the First Embodiment are provided, instead of the pixels, photodetecting elements (not shown) which detect light such as X-rays and convert it to an electrical signal. The scanning lines are driven in the same manner as in the First Embodiment.

[0155]

Inside the photodetector panel 102 where the signal line and the signal processing section 101 are connected is provided a panel switch 107 similar to the signal line switching element SWa of the First Embodiment. The panel switch 107 is controlled so as to sequentially select the blocks, as in the First Embodiment, by the control wire SW_1, etc. (not shown), of the First Embodiment. Note that, here, for convenience of explanation, only a single line and a single panel switch 107 are provided; however, in reality, a plurality of signal lines (s_1, s_2, ... s_N) are connected to a single signal processing section 101 via

their respective panel switches. Further, in reality, as with the sampling circuits of Fig. 5, Fig. 7, and Fig. 9, the signal processing section 101 is provided for the number of signal lines provided in a single block, and each signal processing section is connected to a signal line via the panel switch.

[0156]

The signal processing section 101 therein includes a pre-amplifier (PAMP) 103 which carries out voltage conversion of electrical signals, a main amplifier (MAMP) 104 for amplifying the voltage, and an A/D convertor (ADC) 105 of m bits, and a latch circuit 106 for latching a digital signal of m bits, which are connected in this order.

[0157]

In each line, when the scanning line is switched on and while the line is being selected (one horizontal period), the photodetecting element generates an electrical signal in accordance with the intensity of the received light. The electrical signal is then inputted to the signal processing section 101 through the signal line. The signal processing section 101 carries out voltage conversion of the electrical signal by the pre-amplifier 103, amplifies it in the main amplifier 104, and converts it to a digital signal by the

D/A convertor 105, and after latching it by the latch circuit 106, outputs it to the data storage unit 110. The data storage unit 110 stores the input data.

[0158]

In the foregoing structure, as described in the foregoing embodiments, each panel switch 107 is controlled, for example, in the manner as described in Fig. 2, Fig. 4, and Fig. 21 through Fig. 24, so as to switch the block. Conventionally, in an arbitrary single line, considering a block ("BL1" hereinafter) in which selection has been made and the electrical signal has been generated, and a block ("BL2" hereinafter) which generates and transfers the electrical signal on the signal line after BL1, there are cases where the voltage fluctuates between adjacent signal lines of the respective blocks BL1 and BL2. In contrast, with the structure of the present embodiment, such a fluctuation is prevented by the control as described in the foregoing embodiments, thereby preventing an error on the data which is outputted to the data storage unit 110.

[0159]

Note that, the present invention may have the following arrangement. Namely, the present invention is a

driving method of an active-matrix substrate which includes: a plurality of pixel electrodes which are formed on a substrate; pixel switching elements which are individually connected to the pixel electrodes; a plurality of scanning lines for driving the pixel switching elements; a plurality of signal lines which are connected to the pixel electrodes via the pixel switching elements; a plurality of signal line switching elements which are individually connected at one ends to the plurality of signal lines; a signal input section which is electrically connected to the other ends of the signal line switching elements; a signal line branching section provided between the signal input section and the switching elements; and control wires which are commonly connected per block to the plurality of signal line switching elements and for switching conduction/non-conduction of the signal line switching elements, wherein the potential supplied to the signal lines is inverted to the opposite polarity with respect to a reference potential per predetermined period, and the signal line switching elements of a certain block are conducted with respect to each predetermined period, prior to selecting the signal line switching elements of each block for supplying a desired display signal to the

signal lines and the pixels, and the polarity of the voltage applied to the signal lines here is the same as that of the voltage which is supplied during the select period of the block in the predetermined period with respect to the reference voltage.

[0160]

With this arrangement, since the signal lines are inverted in advance to the opposite polarity, it is possible to prevent the phenomenon in which a potential is applied to the pixels on the border while they are oscillated, which state is then maintained over the display period, thus relieving the drawback of different display states between the border and an area surrounding it, which is caused even when the potentials applied to the border and the surrounding area are the same.

[0161]

Further, the foregoing arrangement may have an arrangement wherein, with respect to each predetermined period, the signal line switching elements of a plurality of blocks are conducted at the same time, prior to selecting the signal line switching elements of each block for supplying the desired display signal to the signal lines and the pixels.

[0162]

With this arrangement, by the provision of a common potential inversion period, it is possible to save time which is required for the polarity inversion, even when driving multiple blocks.

[0163]

Further, the foregoing arrangement may have an arrangement wherein, with respect to each predetermined period, the signal line switching elements of a certain block are conducted prior to selecting the signal line switching elements of each block for supplying the desired display signal to the signal lines and the pixels, and the display signal supplied here in advance to the signal lines corresponds to a half-tone.

[0164]

With this arrangement, the foregoing effect can also be obtained when displaying white, half-tone, or monochromatic color, even though the effect is slightly reduced when displaying black. The foregoing structure and driving method are superior in preventing the border of the blocks from being recognized in a wide range of screens since the visibility on the display with respect to a small change in potential becomes most notable in

half-tone.

[0165]

Further, the present invention is a driving method of an active-matrix substrate which includes: a plurality of pixel electrodes which are formed on a substrate; pixel switching elements which are individually connected to the pixel electrodes; a plurality of scanning lines for driving the pixel switching elements; a plurality of signal lines which are connected to the pixel electrodes via the pixel switching elements; a plurality of signal line switching elements which are individually connected at one ends to the plurality of signal lines; a signal input section which is electrically connected to the other ends of the signal line switching elements; a signal line branching section provided between the signal input section and the switching elements; and control wires which are commonly connected per block to the plurality of signal line switching elements and for switching conduction/non-conduction of the signal line switching elements, wherein the potential supplied to the signal lines is inverted to the opposite polarity with respect to the reference potential per predetermined period, and the signal line switching elements of a certain block are

conducted before the switching elements of an adjacent block which is selected prior to a horizontal period are switched at least to non-conduction.

[0166]

With this arrangement, since the signal lines are inverted to the opposite polarity before the adjacent block becomes non-conducted, it is possible to prevent the phenomenon in which a potential is applied to the pixels on the border while they are oscillated, which state is then maintained over the display period, thus relieving the drawback of different display states between the border and an area surrounding it, which is caused even when the potentials applied to the border and the surrounding area are the same.

[0167]

Further, the present invention is a driving method of an active-matrix substrate which includes: a plurality of pixel electrodes which are formed on a substrate; pixel switching elements which are individually connected to the pixel electrodes; a plurality of scanning lines for driving the pixel switching elements; a plurality of signal lines which are connected to the pixel electrodes via the pixel switching elements; a plurality of signal line

switching elements which are individually connected at one ends to the plurality of signal lines; a signal input section which is electrically connected to the other ends of the signal line switching elements; a signal line branching section provided between the signal input section and the switching elements; and control wires which are commonly connected per block to the plurality of signal line switching elements and for switching conduction/non-conduction of the signal line switching elements, wherein the potential supplied to the signal lines is inverted to the opposite polarity with respect to the reference potential per predetermined period, and the signal line switching elements of a certain block are conducted at least once during a conduction state of the switching elements of the adjacent block which is selected in advance in the predetermined period.

[0168]

With this arrangement, since the polarity inversion is carried out during the selection of the adjacent block, it is possible to prevent the phenomenon in which a potential is applied to the pixels on the border while they are oscillated, which state is then maintained over the display period, thus solving the problem of different display states

at the border of the blocks. Also, the time required for the polarity inversion can be saved.

[0169]

The image display device in accordance with the present invention may be arranged to have the active-matrix substrate which is driven by the foregoing methods. Also, the signal line driving circuit in accordance with the present invention is used for the signal line driving of the image display device having the active-matrix substrate which is driven by the foregoing methods, and may be arranged so that the lines of at least two groups are controlled by different control signals. Further, the signal line driving circuit in accordance with the present invention may have an arrangement wherein the control signal (group control signal) switches the sampling signal. That is, the sampling signal may be switched at the timing of the control signal. Further, the signal line driving circuit in accordance with the present invention may have an arrangement wherein the control signal (group control signal) is equivalent of a transfer signal or a latch signal. That is, data may be transferred or latched at the timing of the control signal.

[0170]

[EFFECTS OF THE INVENTION]

As described above, a data transfer method of the present invention is arranged so that, with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, the blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, respectively, the SL2 is conducted as preliminary conduction within one horizontal period prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

[0171]

This causes a potential hike on the block BL1 by the preliminary conduction and the potential oscillates, which, however, is restored by the subsequent normal conduction by which a correct potential is applied to the BL1. Therefore, this brings about an effect of effectively preventing an error on transfer data, which is caused by the application of a potential to the signal line on the border of the blocks while the signal line is experiencing potential oscillation by the parasitic capacitance between

the signal line and the adjacent signal line.

[0172]

Further, the data transfer method of the present invention is arranged so that, with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, the blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, respectively, a polarity of a potential of the SL2 is inverted as preliminary conduction with respect to the reference voltage within one horizontal period, prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

[0173]

This prevents the phenomenon in which a potential is applied to the pixels on the border while they are oscillated, which state is then maintained over the display period, and therefore brings about an effect of relieving the drawback of different display states between the border and an area surrounding it, which is caused even when the potentials applied to the border and the

surrounding area are the same.

[0174]

Further, the data transfer method of the present invention is arranged so that, in addition to the foregoing arrangement, the signal lines of the plurality of blocks are conducted within the one horizontal period prior to the time the application of the data signal to the BL1 is finished.

[0175]

With this arrangement, even when driving multiple blocks, since the preliminary conduction period such as the preliminary polarity inversion is common to all blocks, the time required for the preliminary inversion does not become overly long as a whole, thus saving time for the normal conduction such as the normal polarity inversion. This allows the signal to be applied without congestion, thus bringing about an effect of improving the quality of data transfer process, in addition to the effect by the foregoing arrangement.

[0176]

Further, the data transfer method of the present invention, in addition to the foregoing arrangement, is arranged so that, during the preliminary conduction of the

BL2, a data signal having intermediate intensity between a maximum value and a minimum value of data signals which are applied to the signal lines is applied to the signal line BL2 which is being preliminarily conducted.

[0177]

With this arrangement, the signal lines in the BL1 will not experience an abrupt potential drop by a small potential difference when the data signal is a half-tone. Therefore, this, in addition to the effect by the foregoing arrangement, brings about an effect of relieving the drawback of different display states between the border and an area surrounding it, which is caused even when the potentials applied to the border and the surrounding area are the same.

[0178]

Further, the data transfer method of the present invention, in addition to the foregoing arrangement, is arranged so that the preliminary conduction of the BL2 is carried out during the normal conduction period of the BL1 within one horizontal period.

[0179]

With this arrangement, even when driving multiple blocks, the time required for the preliminary conduction

such as the preliminary polarity inversion does not become overly long, thus saving time for the normal conduction such as the normal polarity inversion. This allows the signal to be applied without congestion, thus bringing about an effect of improving the quality of data transfer process, in addition to the effect by the foregoing arrangement.

[0180]

Further, the data transfer method of the present invention, in addition to the foregoing arrangement, is arranged so that the preliminary conduction of the BL2 is finished at the time when the normal conduction of the BL1 is finished within one horizontal period, and normal conduction of the BL2 is carried out continuously thereafter.

[0181]

With this arrangement, it is not required to newly create a signal for specifying the start and the end of the preliminary conduction period. Therefore, in addition to the effect by the foregoing arrangement, the arrangement of the device for effecting the foregoing driving can be simplified.

[0182]

Further, the data transfer method of the present invention is arranged so that, when input data of one block, equivalent of n signal lines, which are continuously inputted in a time sequential manner are sampled in n sampling sections and respectively stored as n sampling data, and are outputted to their corresponding signal lines, and when the n sampling sections are divided into groups, and when one of the blocks in which order of sampling the input data with respect to a single scanning line is second or after is BL2, and when a group having a sampling section to which first sampling data Db1 of the block BL2 is inputted is GRa, a blank sampling section for storing the sampling data Db1 is created in the group GRa, after the group GRa stores sampling data of a block in which a sampling time is earlier than the block BL2 with respect to the single scanning line, and before, at the latest, the sampling data Db1 is inputted.

[0183]

With this arrangement, when there are n input lines for the signal lines, it is not required to provide, neither after the nth data signal is sampled nor before the first data signal is sampled again, time for transferring the sampled data signals to the signal lines or latching the

same. Accordingly, it is not required to specially modify the data signals according to the transfer time or latch time. Therefore, data can be transferred rapidly and processed fast with a simpler structure.

[0184]

Further, the data transfer method of the present invention, in addition to the foregoing arrangement, is arranged so that, with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, when a block for which the application of the data signal is finished earlier is BL1, and when a block for which the application of the data signal is finished later is BL2, each of the sampling sections has a plurality of systems for storing the sampling data, and the sampling data of the block BL1 are respectively stored in one of the plurality of systems in each sampling section within a group GR1, and upon finishing the storage, another storage is started in another group with respect to next sampling data, and then the systems are switched in the group GR1 for the next storage to a system which does not currently store data, before storage of sampling data of the block BL2 is started in the group GR1.

[0185]

With this arrangement, even though the storage and output are switched between systems by providing plural systems with respect to each signal line within a block, the group which performs the storage process is switched to ensure sampling of the data signal in another group, thus surely preventing failure to pick up data. Therefore, in addition to the effect by the foregoing arrangement, data can be transferred faster with a simpler arrangement, thereby bringing about an effect of processing data at high speed.

[0186]

Further, the data transfer system of the present invention, in addition to the foregoing arrangement, is arranged so that when a group GR1 is one of the groups, the sampling data stored in the group GR1 are outputted after it was stored at least in the group GR1, and while storing sampling data in another group.

[0187]

With this arrangement, even though the storage and output are switched between systems by providing plural systems with respect to each signal line within a block, the group which performs the storage process is switched to ensure sampling of the data signal in another group,

thus surely preventing failure to pick up data. Therefore, in addition to the effect by the foregoing arrangement, data can be transferred faster with a simpler arrangement, thereby bringing about an effect of processing data at high speed.

[0188]

Further, the data transfer method of the present invention is arranged so that, with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, the blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, respectively, the application of the data signal to the SL2 is started within one horizontal period, prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

[0189]

With this arrangement, the block BL1 experiences the potential hike and the potential oscillates. However, normal conduction is carried out thereafter so as to apply

the correct potential to BL1 and thereby restore the potential oscillates. Therefore, it is possible to effectively prevent an error on transfer data, which is caused by the application of a potential to the signal line on the border while the signal line is experiencing potential oscillation by the parasitic capacitance between the signal line and the adjacent signal line.

[0190]

Further, the data transfer method of the present invention is for an image display device and is arranged so that, with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, among which a block for which the application of the data signal is finished earlier is BL1, and a block for which the application of the data signal is finished later is BL2, the blocks BL1 and BL2 having adjacent signal lines SL1 and SL2, respectively, the application of the data signal to the SL2 is started within one horizontal period, prior to the time the application of the data signal to the BL1 is finished as normal conduction for applying the data signal.

[0191]

With this arrangement, the block BL1 experiences

the potential hike and the potential oscillates. However, normal conduction is carried out thereafter so as to apply the correct potential to BL1 and thereby restore the potential oscillates. Therefore, in a display device, it is possible to relieve the drawback of different display states between the border and an area surrounding it, the drawback being caused by the application of a potential to the signal line on the border while the signal line is experiencing potential oscillation by the parasitic capacitance between the signal line and the adjacent signal line, the drawback being caused even when the potentials applied to the border and the surrounding area are the same.

[0192]

An image display device of the present invention is arranged so that the data signal is transferred from the data transfer section to the pixels on the matrix using any of the foregoing data transfer methods.

[0193]

With this arrangement, it is possible to prevent the phenomenon in which a potential is applied to the pixels on the border while they are oscillated, which state is then maintained over the display period. Therefore, it is

possible to relieve the drawback of different display states between the border and an area surrounding it, which is caused even when the potentials applied to the border and the surrounding area are the same.

[0194]

Further, a signal line driving circuit of the present invention is for the image display device and is arranged so that, when input data of one block, equivalent of n signal lines, which are continuously inputted in a time sequential manner are sampled in n sampling sections and respectively stored as n sampling data, and outputted to their corresponding signal lines, and when the n sampling sections are divided into groups, and when one of the blocks in which order of sampling the input data with respect to a single scanning line is second or after is BL2, and when a group having a sampling section to which first sampling data Db1 of the block BL2 is inputted is GRa, the signal line driving circuit generates a group control signal for specifying a timing of creating a blank sampling section for storing the sampling data Db1 in the group GRa, after the group GRa stores sampling data of a block in which a sampling time is earlier than the block BL2 with respect to a single scanning line, and before, at

the latest, the sampling data Db1 is inputted.

[0195]

With this arrangement, when there are n input lines for the signal lines, it is not required to provide, neither after the nth data signal is sampled nor before the first data signal is sampled again, time for transferring the sampled data signals to the signal lines or latching the same. Accordingly, it is not required to specially modify the data signals according to the transfer time or latch time. Therefore, data can be transferred rapidly and processed fast with a simpler structure.

[0196]

Further, the signal line driving circuit of the present invention, in addition to the foregoing arrangement, is arranged so that with respect to at least one pair of the blocks respectively having signal lines which are adjacent to each other, when a block for which the application of the data signal is finished earlier is BL1, and when a block for which the application of the data signal is finished later is BL2, each of the sampling sections has a plurality of systems for storing the sampling data, and the sampling data of the block BL1 are respectively stored in one of the plurality of systems in each sampling section

within a group GR1, and upon finishing the storage, and before another storage is started in another group with respect to next sampling data, the signal line driving circuit generates a signal as the group control signal for specifying a timing of switching the systems in the group GR1 for the next storage to a system which does not currently store data, before storage of sampling data of the block BL2 is started in the group GR1.

[0197]

With this arrangement, even though the storage and output are switched between systems by providing plural systems with respect to each signal line within a block, the group which performs the storage process is switched to ensure sampling of the data signal in another group, thus surely preventing failure to pick up data. Therefore, in addition to the effect by the foregoing arrangement, data can be transferred faster with a simpler arrangement, thereby bringing about an effect of processing data at high speed.

[0198]

Further, the data signal line driving circuit of the present invention, in addition to the foregoing arrangement, is arranged so that when a group GR1 is one

of the groups, the signal line driving circuit generates a signal as the group control signal for specifying a timing of outputting the sampling data stored in the group GR1, after it was stored at least in the group GR1, and while storing sampling data in another group.

[0199]

With this arrangement, it is not required to switch the storage and output between the systems by providing plural systems with respect to each signal line within a block, and it is not required to provide time for switching. Therefore, in addition to the effect by the foregoing arrangement, data can be transferred faster with a simpler arrangement, thereby bringing about an effect of processing data at high speed.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1]

An explanatory drawing showing an equivalent circuit of an active-matrix substrate.

[Fig. 2]

An explanatory drawing showing a timing chart by a driving method employing the active-matrix substrate.

[Fig. 3]

An explanatory drawing showing a display state of a

liquid crystal display device using the active-matrix substrate of Fig. 1.

[Fig. 4]

An explanatory drawing showing a timing chart by the driving method employing the active-matrix substrate.

[Fig. 5]

A block diagram showing an exemplary structure of a signal line driving circuit.

[Fig. 6]

An explanatory drawing showing a timing chart of the signal line driving circuit of Fig. 5.

[Fig. 7]

A block diagram showing an exemplary structure of a signal line driving circuit.

[Fig. 8]

An explanatory drawing showing a timing chart of the signal line driving circuit of Fig. 7.

[Fig. 9]

A block diagram showing an exemplary structure of a signal line driving circuit.

[Fig. 10]

An explanatory drawing showing a timing chart of the signal line driving circuit of Fig. 9.

[Fig. 11]

A block diagram showing a schematic exemplary structure of a conduction controlling section.

[Fig. 12]

A block diagram showing a schematic exemplary structure of a conduction controlling section.

[Fig. 13]

A block diagram showing a schematic exemplary structure of a circuit for generating a group control signal and a control signal.

[Fig. 14]

A block diagram showing a schematic exemplary structure of an output buffer.

[Fig. 15]

A block diagram showing a schematic exemplary structure of an output buffer.

[Fig. 16]

A block diagram showing a schematic exemplary structure of a D/A convertor.

[Fig. 17]

A block diagram showing a schematic exemplary structure of a D/A convertor.

[Fig. 18]

A block diagram showing an exemplary structure of a signal line driving circuit.

[Fig. 19]

An explanatory drawing showing a timing chart of the signal line driving circuit of Fig. 18.

[Fig. 20]

An explanatory drawing showing an exemplary structure for applying an image signal to signal lines by dividing the signal lines into two or more blocks.

[Fig. 21]

An explanatory drawing showing a timing chart by the driving method employing the active-matrix substrate.

[Fig. 22]

An explanatory drawing showing a timing chart by the driving method employing the active-matrix substrate.

[Fig. 23]

An explanatory drawing showing a timing chart by the driving method employing the active-matrix substrate.

[Fig. 24]

An explanatory drawing showing a timing chart by the driving method employing the active-matrix substrate.

[Fig. 25]

A block diagram showing a schematic exemplary

structure of a photodetector.

[Fig. 26]

An explanatory drawing showing a timing chart by the driving method employing a conventional active-matrix substrate.

[REFERENCE NUMERALS]

1 Signal line driving circuit (data transfer section)

2 Scanning line driving circuit

3, 4, 5 Display areas

7 Signal line branching section

11 First block

12 Second block

15, 16, 17, 18, 19, 20 Sampling circuit

21 PLL oscillator

22 H counter

23 SW_1 decoder

24 SW_2 decoder

31 H counter

32 SW_1 decoder

33 SW_2 decoder

41 H counter

42 V counter

43 CNT decoder

44 CNTa decoder

45 CNTb decoder

51 OP amplifier

52 Switch

53 Level shifter

61 D/A convertor

62 Switch

63 Level shifter

71, 72 Sampling circuit

101 Signal processing section (data transfer section)

102 Photodetector panel

107 Panel switch

103 Pre-amplifier

104 Main amplifier

105 A/D convertor

106 Latch circuit

110 Data storage unit

a, b, c, d, e, e', f, f' Signal line

A_1, B_1, C_1, D_1, A_2, B_2, C_2, D_2 Pixel

ASWA, ASWB, ASWC, ASWD, ASWS, ASWH Analog switch

Bu Output buffer

CLK Clock

CNTa, CNTb Group control signal

CNT, CNT0 Control signal

Csd Parasitic capacitance

C_{SHA}, C_{SHB} Sampling hold capacitor

C_S Sampling capacitor

C_H Holding capacitor

DAC D/A convertor

DAT data line

g_1, g_2 Scanning line

HSY Horizontal synchronize signal

LSa, LSb Group control signal

RL Base potential

s_1, s_2, s_3, s_4 Output line

SAM_1, SAM_n Sampling line

SW_1, SW_2 Control wire

Swa, SWb, SWc, SWd Signal line switching element

Vd Charge voltage

VSY Vertical synchronize signal

[TITLE OF THE DOCUMENT] ABSTRACT

[ABSTRACT]

[OBJECT] When transferring data per block, the problem of different potential states between the border of the blocks and an area surrounding it, which is caused by the potential oscillation of the signal line on the border of the blocks, is relieved.

[MEANS TO ACHIEVE THE OBJECT] Each signal line enters a preliminary polarity inversion period prior to a normal polarity inversion period so as to be inverted to the opposite polarity. By the preliminary polarity inversion a signal line on a border of blocks experiences a potential hike and the potential oscillates, which, however, is restored later by the application of a correct potential in the normal polarity inversion period.

[SELECTED DRAWINGS] Fig. 2